EXHIBIT 2

U.S. Patent No. 8,549,339 ("'339 Patent")

Accused Products: Qualcomm's products comprising one or more SoC each comprising two or more sets of processors implementing or based on the DynamIQ Shared Unit architecture or big.LITTLE architecture, including without limitation: SM4250-AA (Snapdragon 460), SM4350 (Snapdragon 480), SM4350-AC (Snapdragon 480+), SM4375 (Snapdragon 4 Gen 1), SM4450 (Snapdragon 4 Gen 2, Snapdragon 4 Gen 2 Accelerated Edition), SM4635 (Snapdragon 4s Gen 2), DM630 (Snapdragon 630), SDM632 (Snapdragon 632), SDM636 (Snapdragon 636), MSM8956 (Snapdragon 650), MSM8976 (Snapdragon 652), MSM8976 Pro (Snapdragon 653), SDM660/SDA660 (Snapdragon 660), SM6115 (Snapdragon 662), SM6125 (Snapdragon 665), SDM670 (Snapdragon 670), SM6150 (Snapdragon 675), SM6150-AC (Snapdragon 678), SM6225 (Snapdragon 680), SM6225-AD (Snapdragon 685), SM6350 (Snapdragon 690), SM6375 (Snapdragon 695), SM6450 (Snapdragon 6 Gen 1), SM6115-AC (Snapdragon 6s Gen 1), SM6475-AB (Snapdragon 6 Gen 3), SM6375-AC (Snapdragon 6s Gen 3), SDM710 (Snapdragon 710), SDM712 (Snapdragon 712), SM7125 (Snapdragon 720G), SM7150-AA, (Snapdragon 730), SM7150-AB (Snapdragon 730G), SM7150-AC (Snapdragon 732G), SM7225 (Snapdragon 750G), SM7325 (Snapdragon 778G), SM7325-AE (Snapdragon 778G+), SM7350-AB (Snapdragon 780G), SM7325-AF (Snapdragon 782G), SM7435-AB (Snapdragon 7s Gen 2), SM7550-AB (Snapdragon 7 Gen 3), SM7675-AB (Snapdragon 7+ Gen 3), SM7635 (Snapdragon 7s Gen 3), MSM8992 (Snapdragon 808), MSM8994 (Snapdragon 810), MSM8994v2 (Snapdragon 810), MSM8994v2.1 (Snapdragon 810), MSM8996Lite (Snapdragon 820), MSM8996 (Snapdragon 820), MSM8996Pro-AB (Snapdragon 821), MSM8996Pro-AC (Snapdragon 821), MSM8998 (Snapdragon 835), SDM845 (Snapdragon 845), SM8150 (Snapdragon 855), SM8150-AC (Snapdragon 855+), SM8150-AC (Snapdragon 860), SM8150P (Snapdragon 855+), SM8250 (Snapdragon 865), SM8250-AB (Snapdragon 865+), SM8250-AC (Snapdragon 870), SM8350 (Snapdragon 888), SM8350-AC (Snapdragon 888+), SM8450 (Snapdragon 8 Gen 1), SM8475 (Snapdragon 8+ Gen 1), SM8425-100-AC (Snapdragon 8+ Gen 1 4G), SM8550-AB (Snapdragon 8 Gen 2), SM8550-AC (Snapdragon 8 Gen 2 for Galaxy), SM8650-AB (Snapdragon 8 Gen 3), SM8650-AC (Snapdragon 8 Gen 3 for Galaxy), SM8635 (Snapdragon 8s Gen 3), MSM8998 (Snapdragon 835 Mobile PC Platform), SDM850 (Snapdragon 850 Mobile Compute Platform), SC7180 (Snapdragon 7c), SC7180P (Snapdragon 7c Gen 2), SC7280 (Snapdragon 7c+ Gen 3), SC8180 (Snapdragon 8c), SC8180X (Snapdragon 8cx), SC8180XP (Snapdragon 8cx Gen 2), SC8280 (Snapdragon 8cx Gen 3), MSM8996AU (Snapdragon 820A), SA6155P, SA8155P (Snapdragon 855A), SA8195P, SA8255P, SA8295P, APQ8094 (Snapdragon 810E), APQ8096 (Snapdragon 820E), QCS603, QCS605, XR1, XR2, XR2+ Gen 1, XR2 Gen 2, XR2+ Gen 2, G3x Gen 1, G3x Gen 2, SQ1, SQ2, and SQ3.

Each Accused Product infringes the claims in substantially the same way, and the evidence shown in this chart is similarly applicable to each Accused Product. For example, each Accused Product includes a DynamIQ Shared Unit or big.LITTLE architecture and, on information and belief, implements substantially the same architectural features described in the reference documentation cited in this chart. Thus, the descriptions and evidence below relating to the Snapdragon 8 Gen 2 Octa-Core and Snapdragon 835 Mobile Platform representative products are similarly applicable to the remaining Accused Products listed above (for DynamIQ and big.LITTLE architectures respectively). Each claim limitation is literally infringed by each Accused Product. However, to the extent any claim

limitation is not met literally, it is nonetheless met under the doctrine of equivalents because the differences between the claim limitation and each Accused Product would be insubstantial, and each Accused Product performs substantially the same function, in substantially the same way, to achieve the same result as the claimed invention. Notably, Qualcomm has not yet articulated which, if any, particular claim limitations it believes are not met by the Accused Products

Claim 1

Claim 1	Accused Products
[1pre] 1. A multi-core processor, comprising:	To the extent the preamble is limiting, each Accused Product comprises a multi-core processor. For example, Snapdragon 8 Gen 2 Octa-Core processor, designated QCS8550 with die code name Kailua, *see* Defendants' Objections and Responses to Redstone Logics LLC's First Set of Interrogatories Nos. 1-15 ("ROG Responses") at 15, contains eight cores implementing the ARM DynamIQ Shared Unit-110 architecture. In a further example, the Snapdragon 835 Mobile Platform contains eight cores implementing the ARM big.LITTLE architecture. *See, e.g.*:

Claim 1	Accused Products

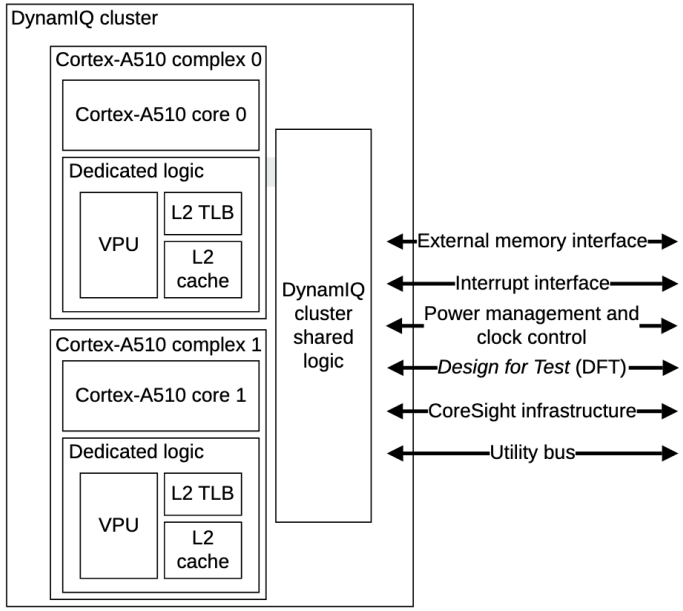
	Snapdragon 8 Gen 2 (2023) [edit]
	The **Snapdragon 8 Gen 2** was announced on November 15, 2022.[252]
	Notable features over its predecessor (8 Gen 1):
	• 4nm (TSMC N4) process
	• Support up to 16 GB LPDDR5X 4200 MHz
	• Support UFS 4.0
	• CPU features
	  • 1 Kryo Prime (ARM Cortex-X3), up to 3.36 GHz. Prime core
	  • 1MB L2 cache
	  • Only 64-bit support [253]
	  • 2 Kryo Gold (ARM Cortex-A715), up to 2.8 GHz. High Performance cores
	  • Only 64-bit support [253]
	  • 2 Kryo Gold (ARM Cortex-A710), up to 2.8 GHz. Performance cores
	  • 32-bit and 64-bit support[253]
	  • 3 Kryo Silver (ARM Cortex-A510), up to 2 GHz. Efficiency cores
	  • 32-bit and 64-bit support[253]
	  • 35% performance uplift and 40% power efficiency improvement
	  • 8 MB system-level cache
	https://en.wikipedia.org/wiki/List_of_Qualcomm_Snapdragon_systems_on_chips#Snapdragon_8_Gen_2_(2023)

<table>
<tr><th>Claim 1</th><th>Accused Products</th></tr>
<tr><td></td><td>
<table>
<tr><th>Model number</th><th>Product Name</th><th>Fab</th><th>Die size</th><th>CPU</th></tr>
<tr><td>MSM8998[246]</td><td>Snapdragon 835</td><td>10 nm FinFET (Samsung 10LPE)</td><td>72.3 mm^2</td><td>4 + 4 cores Kryo 280 (2.45 GHz Cortex-A73 + 1.9 GHz Cortex-A53)</td></tr>
</table>
https://en.wikipedia.org/wiki/List_of_Qualcomm_Snapdragon_systems_on_chips#Snapdragon_800_series_(2013%E2%80%932021)
</td></tr>
</table>

Claim 1	Accused Products
	DynamIQ Shared Unit-110 First DynamIQ Shared Unit of the Armv9 generation, up to 12 cores supported, up to 16MB L3, and enhanced power management features. **Supporting:** • Cortex-X3 • Cortex-X2 • Cortex-A715 • Cortex-A710 • Cortex-A510 https://www.arm.com/technologies/dynamiq

Claim 1	Accused Products

Figure 2-2: Example configuration with two Cortex®-A510 single-core complexes

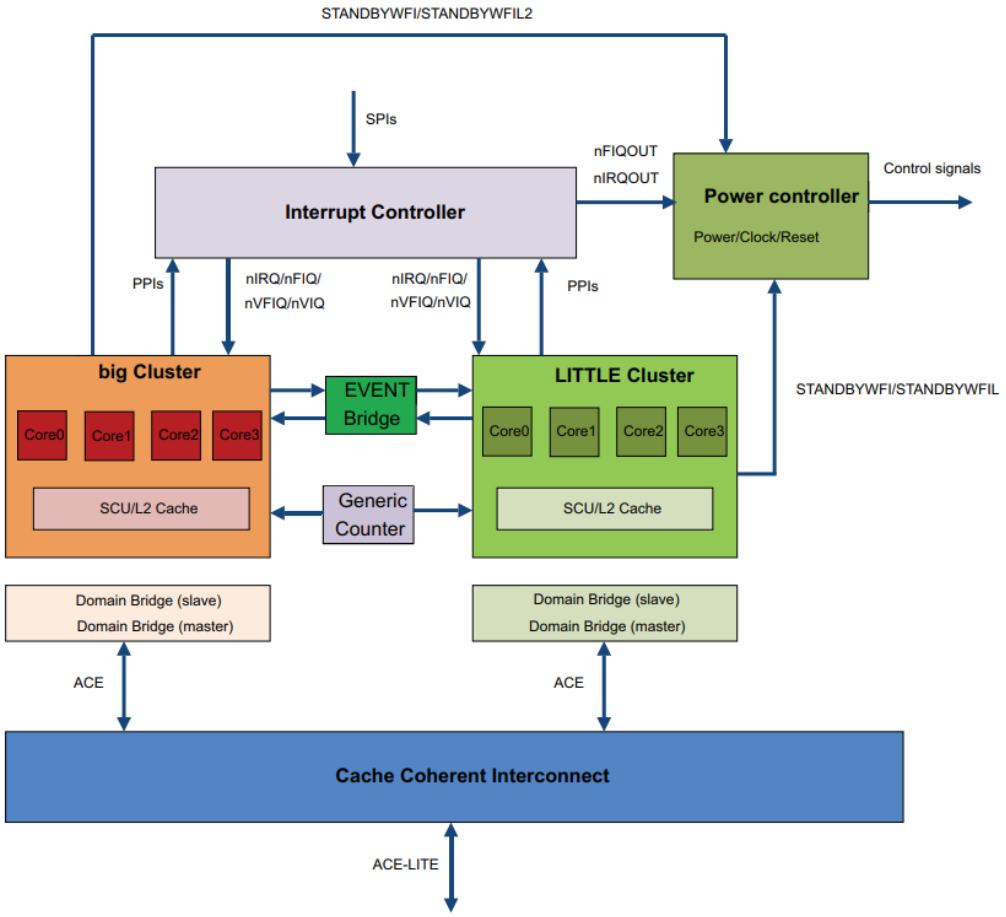


Arm Cortex-A510 Core Technical Reference Manual at p. 23

> Our initial testing shows that Snapdragon 835's Kryo 280 CPU is an octa-core, big.LITTLE configuration with four semi-custom A73 "performance" cores and four semi-custom A53 "efficiency" cores. Kryo 280's performance cores are pretty much equivalent to Kirin 960's A73 cores in both integer and floating-point IPC, but comparing them to Snapdragon 820's Kryo CPU shows mixed results: integer IPC improves but floating-point regresses.

https://www.anandtech.com/show/11201/qualcomm-snapdragon-835-performance-preview/6

Claim 1	Accused Products
	1.2 Document scope This application note focuses on the following processors and highlights important issues when powering up or powering down processor cores and clusters on an SoC. • Cortex®-A7. • Cortex®-A15. • Cortex®-A17. • Cortex®-A53. • Cortex®-A57. • Cortex®-A72. • Cortex®-A73. "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/ **2.1 ARM® big.LITTLE™ system example** A big.LITTLE system uses two different types of cores that are combined in a coherent system. big cores are designed for high performance while LITTLE cores are designed for high energy efficiency. The big cores are used for resource-intensive software threads, and energy-efficient LITTLE cores handle low-intensity software threads that use fewer compute resources. The result is high energy efficiency and high performance. "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products
	 **Figure 2-1 A typical big.LITTLE system** "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

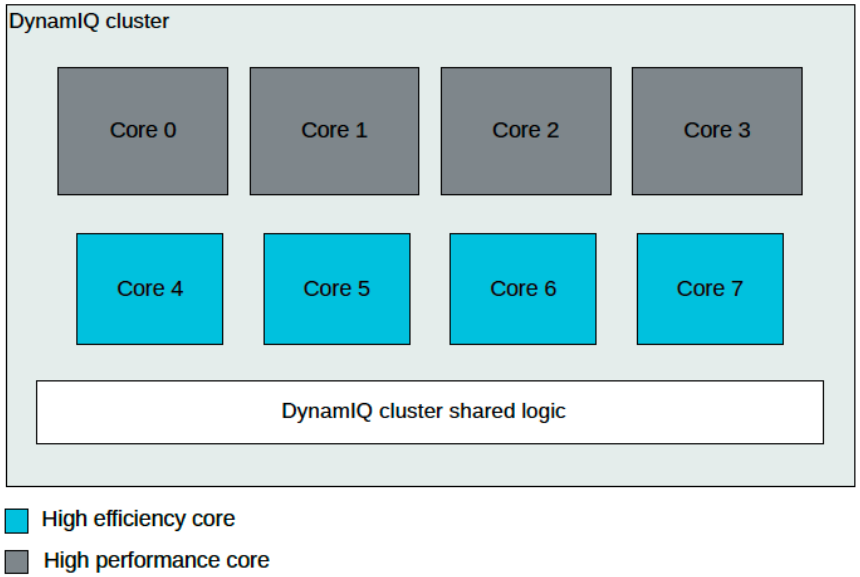
Claim 1	Accused Products
[1a] a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input;	Each Accused Product comprises a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input. For example, the Snapdragon 8 Gen 2 Octa-Core includes a first set of high efficiency processor cores (two or more ARM Cortex-A510 cores). The processor cores in the first set receive a dynamic supply voltage and a first output clock signal of a first PLL having a first clock signal as input. For another example, the Snapdragon 835 Mobile Platform includes a first set of high efficiency processor cores (two or more A53 cores). The processor core(s) in the first set receive a dynamic supply voltage and a first output clock signal of a first PLL having a first clock signal as input. ARM documentation for the big.LITTLE and DynamIQ architectures used in the Accused Products directly shows that each core cluster receives its own clock domain. At the time the Accused Products were designed, it was typical to produce this clock using a PLL that has a corresponding clock input. Furthermore, ARM documentation for an earlier, related device (the Cortex-A15_A7 MPCore test chip, which also has independent clock domains for different CPU clusters) shows each CPU cluster receiving an output clock signal from a PLL having a corresponding clock signal as input (*e.g.* from an oscillator). *See, e.g.*:

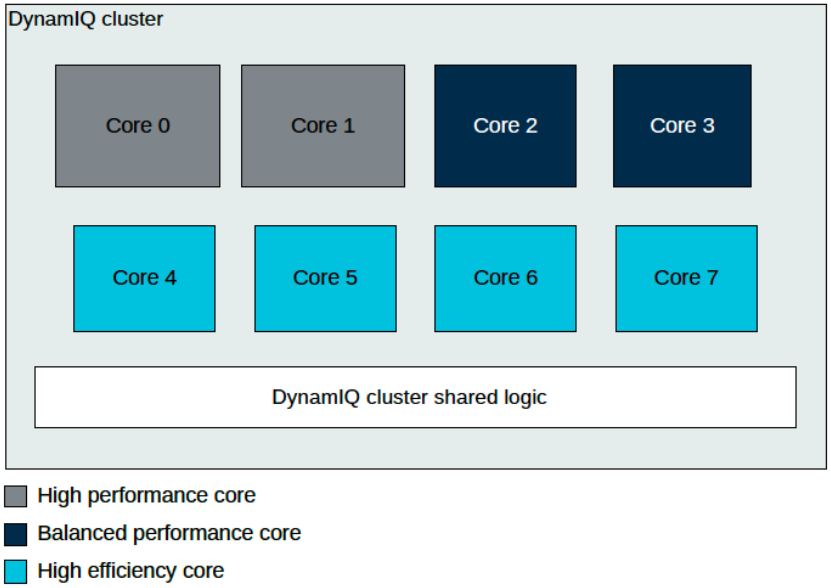
Claim 1	Accused Products

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	Notable features over its predecessor (8 Gen 1):
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	  • 35% performance uplift and 40% power efficiency improvement
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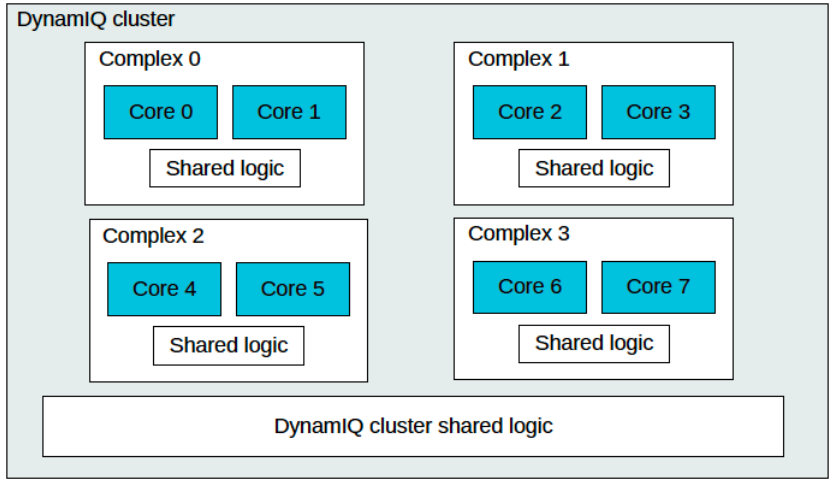
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</td></tr>
</table>

Claim 1	Accused Products
	Cluster features The DSU-110 has the following cluster features: • Support for Arm®v9.0-A architecture cores • Support for up to four types of core, and a maximum of 12 cores in the cluster • *Power Policy Units* (PPUs) providing autonomous power management of the L3 cache and the cores • Support for cores running independently at different frequencies and voltages known as *Dynamic Voltage Frequency Scaling* (DVFS). For cores in a complex, DVFS is only possible for the whole complex not for individual cores. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual, available at https://documentation-service.arm.com/static/62bb28beb334256d9ea8cc32, at p. 19 A cluster can be configured with up to four different types of cores in the same cluster. Each core type targeting different power efficiency and performance levels. This arrangement allows for an intermediate core that has an intermediate performance and efficiency level. The cluster also supports complexes. A cluster can be configured in many arrangements. Examples of cluster arrangements are: • One or more cores of the same type. • Various arrangements of two types of cores. For example, one or more cores targeting either a high-performance level or a higher power efficiency level. • Various arrangements of three or four types of cores. For example, one or more high-peformance cores, power-efficient cores, and intermediate cores. • One or more complexes and no individual cores. For information on complexes, see 2.3.1 What is a complex? on page 25. • One or more complexes and individual cores. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 22

Claim 1	Accused Products
	 Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 23

Claim 1	Accused Products
	 Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 24

Claim 1	Accused Products



Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 24

The DSU-110 DynamIQ™ cluster supports blocks that are called complexes which contain up to two cores of the same type and some shared logic. Sharing some logic between the two cores of a dual core complex can make the dual core complex area efficient. However, this area efficiency is at the cost of reduced performance compared with using two single-core complexes.

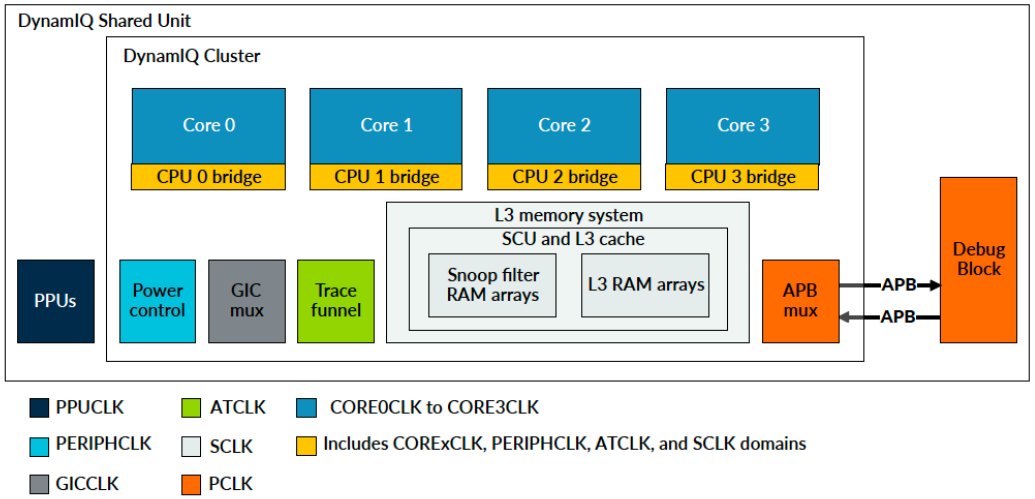
Arm® DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 25

Claim 1	Accused Products

The *DynamIQ™ Shared Unit-110* (DSU-110) has multiple clock domains. Each core or complex can be implemented in a separate clock domain.

The following figure shows the clock domains for an example cluster with four standalone cores.

Figure 4-1: DSU-110 clock domains



Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 46

The *DynamIQ™ Shared Unit-110* (DSU-110) *Power Policy Units* (PPUs) control power management for the Cortex®-A510 core. A Cortex®-A510 complex supports separate gated power domains for the complex, for each core inside the complex, and for the *Vector Processing Unit* (VPU). It also supports a dedicated voltage domain for each complex, and a voltage domain for the DSU-110 DynamIQ™ cluster.

Arm Cortex-A510 Core Technical Reference Manual at p. 39

Claim 1	Accused Products
	The cluster contains several clock domains for functionality that is likely to be connected to different clocks in the system. Within each core, the CPU bridge contains asynchronous bridges fo all crossings between the core and cluster clock domains. Each CPU bridge is split, with one half of each bridge in the core clock domain and the other half in the relevant cluster domain. At the cluster level, there is the *Snoop Control Unit* (SCU) bridge which contains crossings between the cluster clock domains as required. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 46 The DynamIQ Shared Unit-110 (DSU-110) has a separate clock signal for each standalone core or complex. There are also separate clocks for the internal logic, and some of the e interfaces. The following table describes the clock signals of the DSU-110. *Table 1. DSU-110 clock signals* **Signal** / **Description** COREyCLK: The clocks for each of the cores in the cluster that are not part of a complex. y is the core instance number, for example, CORE0CLK is the clock for core 0. These signals clock all core logic, including L1 and L2 caches. COMPLEXxCLK: The clocks for each complex in the cluster. Each clock is connected to all cores in the respective complex. x is the complex instance number, for example, COMPLEX0CLK is the clock for complex 0. https://developer.arm.com/documentation/101381/0400/Clocks-and-resets/Clocks-

Claim 1	Accused Products

4.1.1 Input clocks

Input clocks must be provided with a source that is external to, or embedded in, the subsystem.

Table 4-1: Input clocks

Clock	Description
REFCLK	Main reference clock The input clock to *System Control Processor* (SCP) boots coming out of reset. REFCLK also clocks other logic like SCP generic and watchdog timers.
CPUxPLLCLKn	CPUxPLLCLKn is a high-frequency reference clock inputs used for application core PLL, that is, one per core, where n = 0-7.
CLUS0PLLCLKn	CLUS0PLLCLKn is a high-frequency reference clock inputs used for cluster PLL, that is, one clock per cluster, where n is the number of clusters in a subsystem. As RD-TC21 reference subsystem only contain one cluster, n is fixed to 1.
INTPLLCLK	INTPLLCLK is a high-frequency reference clock input used for the Interconnect block.
SYSPLLCLK	SYSPLLCLK is a high-frequency clock input for the main block.
DMCPLLCLK	DMCPLLCLK is a high-frequency reference clock input used for the Memory block.
GPUPLLCLK	GPUPLLCLK is a high-frequency reference clock input used for the GPU block.

Arm® Total Compute 2021 Reference Design Software Developer Guide at p. 40

4.1.2 Systems clocks

RD-TC21 internally derives clocks that are used for parts of the subsystem. These clocks are generated only when the VSYS.SYSTOP power domain is powered. Each clock can be individually controlled.

The following table summarizes these derived internal clocks.

Id.

Claim 1	Accused Products

Table 4-2: Systems internal derived clocks

Clock Signal	PLL	Description
CLUSxCORECLKn n is the number of clusters in a subsystem.	CPUPLL	Core clock. Each core is clocked independently to each other. Therefore, One clock per cluster, where
CLUSxCLK	CLUSxPLLCLKn	CPU Cluster x clock. The cluster clock drives the logic in the Processor block, where x is 0 to 31.
INTCLKOUT	INTPLLCLK	Coherent Interconnect Clock Clock for the interconnect and other expansion master and slave ports. This clock is generated from INTPLLCLK

Id. at p. 41

4.3 Power control

Good power management is key to reduce system power consumption while maintaining a high performance.

An RD-TC21 reference subsystem contains the following power management features:

- Multiple voltage domains to allow for *Dynamic Voltage and Frequency Scaling* (DVFS) on application processors and the GPU
- Multiple power-gated regions provide comprehensive leakage management
- Multiple power modes for different system scenarios
- A *System Control Processor* (SCP) based on a Cortex®-M3 processor controls power, clock, reset, and the static configuration of the system
- *Power Policy Units* (PPUs) are used to manage power states of each voltage and power domain under the control of the SCP

Id. at 47-48

Claim 1	Accused Products
	4.3.1 Voltage domain A voltage domain is defined as a collection of design elements supplied by a single voltage. The voltage supply to the domain might be scaled or switched off for power or performance reasons. Total Compute 2021 Reference Design (RD-TC21) supports the following voltage domains: **VCPU0** The first voltage domain in the processor cluster for "LITTLE" cores. Supports DVFS. **VCPU1** The second voltage domain in the processor cluster for ELP and "big" cores. Supports DVFS. **VGPU** The voltage domain for GPU. Supports DVFS. **VSYS** The voltage domain for the rest of the subsystem. Does not support DVFS. *Id.* at p. 48 **SCP runtime firmware** The SCP runtime firmware executes after *Trusted Firmware for A-profile* (TF-A) BL2 has authenticated and copied it from flash. The SCP runtime firmware performs the following functions: • Responds to *System Control and Management Interface* (SCMI) messages through *Message Handling Unit* (MHU) version 2.0 for processor power control and *Dynamic Voltage and Frequency Scaling* (DVFS) • Power domain management • Clock management *Id.* at p. 65

Claim 1	Accused Products
	Our initial testing shows that Snapdragon 835's Kryo 280 CPU is an octa-core, big.LITTLE configuration with four semi-custom A73 "performance" cores and four semi-custom A53 "efficiency" cores. Kryo 280's performance cores are pretty much equivalent to Kirin 960's A73 cores in both integer and floating-point IPC, but comparing them to Snapdragon 820's Kryo CPU shows mixed results: integer IPC improves but floating-point regresses. https://www.anandtech.com/show/11201/qualcomm-snapdragon-835-performance-preview/6 **Voltage domains** The voltage supply to a domain might be scaled or removed for power or performance reasons. Except for low complexity solutions, it is rare to use a single logic voltage supply for the whole SoC. The primary reason for additional voltage domains is to support DVFS for functional areas of the SoC. The second reason is to enable external supply switch-off, or reduction to non-functional state retention levels, to some logic areas while maintaining an operational level supply to others. However, the cost for additional voltage domains is significant, because additional voltage regulators, extra effort, and complexity are required in the SoC physical implementation. Therefore, you must carefully assess the value of the addition of each voltage domain against the performance and power requirements for the design. In a big.LITTLE system, each cluster must have a dedicated voltage supply. This is a critical success factor when combined with big.LITTLE software. "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products

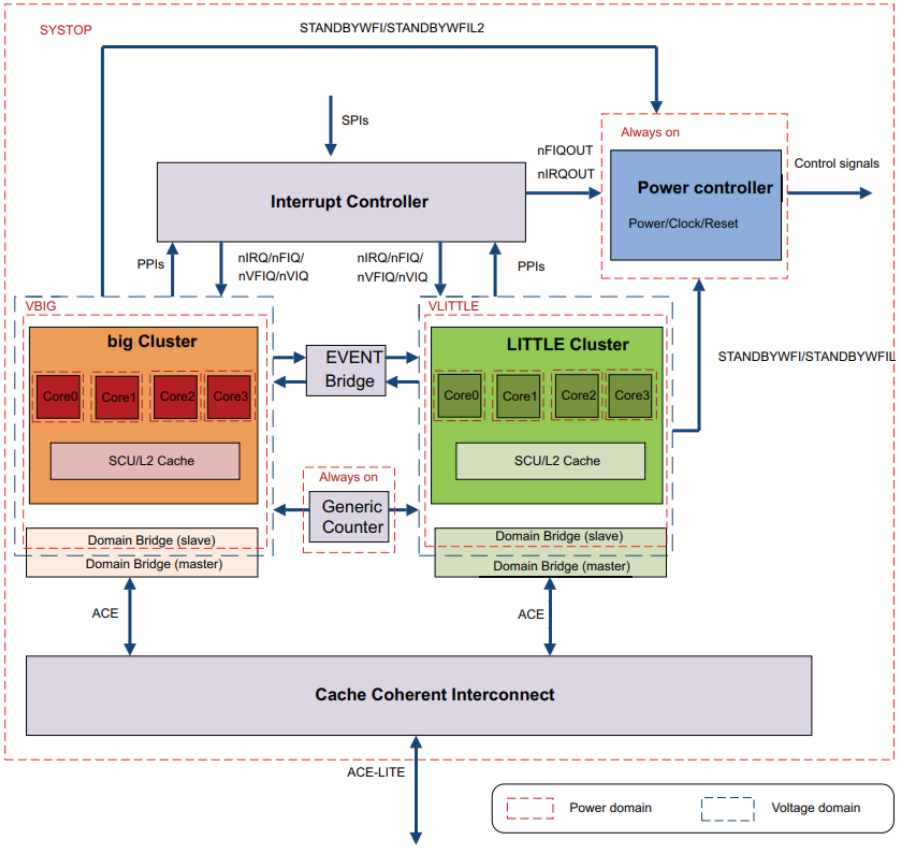
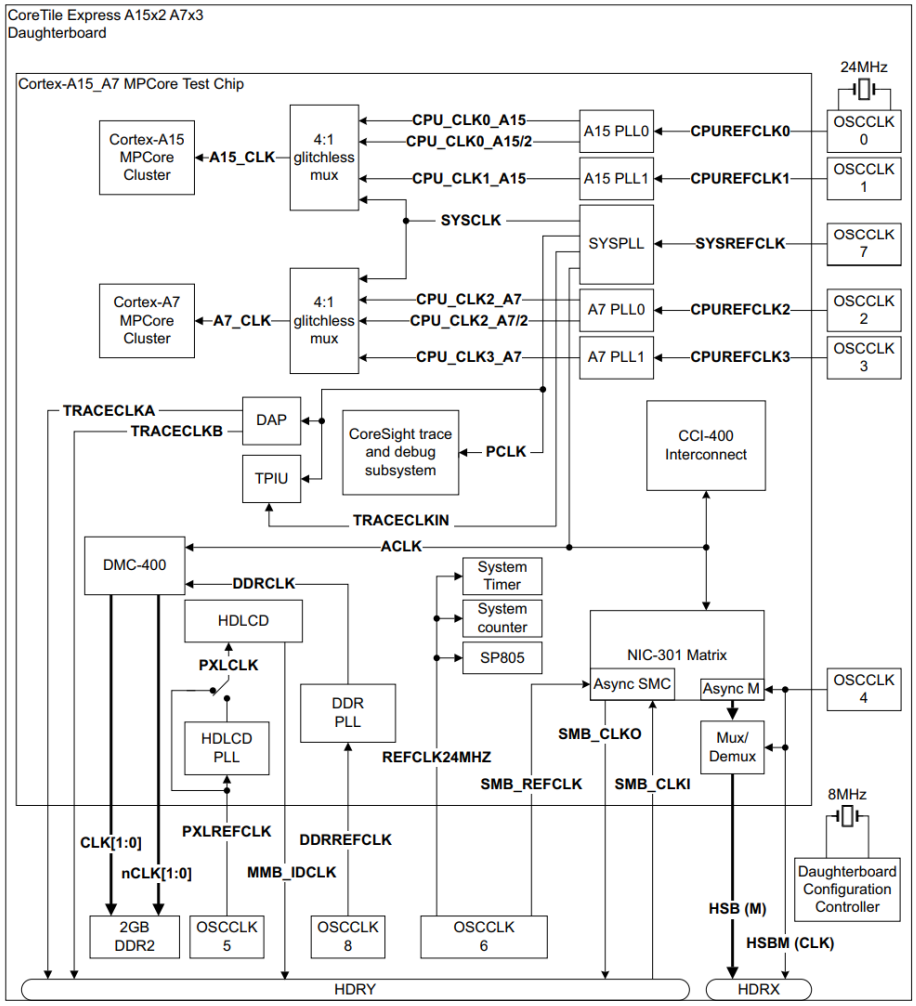


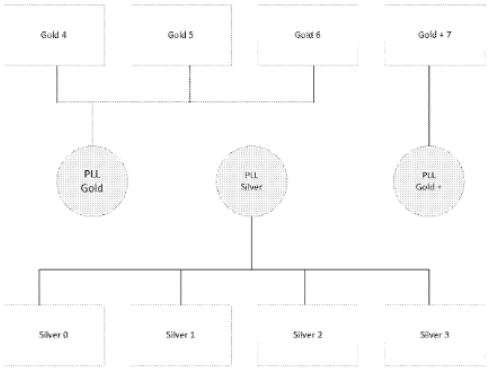
Figure 2-2 Power domain hierarchy

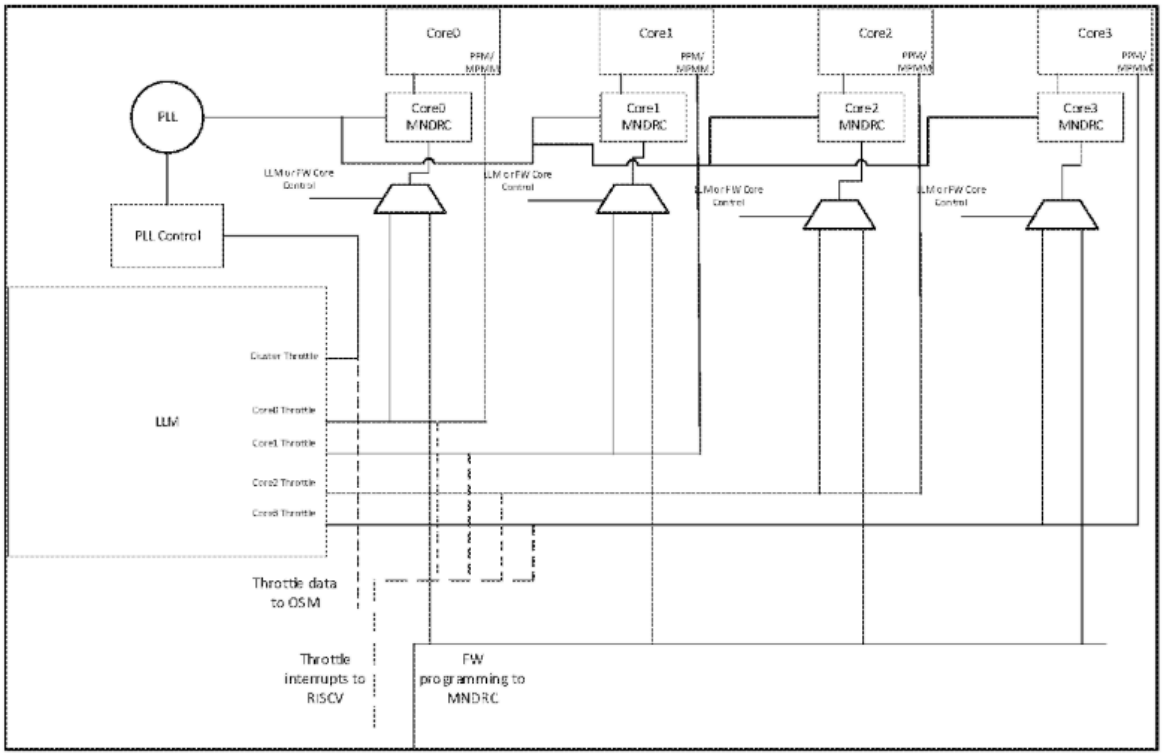
In Figure 2-2, two processor clusters are implemented with per-core and cluster power domains. The big cluster is in the VBIG voltage domain, while the LITTLE cluster is in the VLITTLE voltage domain. The system controller is in an always-on power domain. All the other components are in the system logic power domain (SYSTOP).

"High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products
	Clock domains Clock domains can interact with each other synchronously or asynchronously. Synchronous clock domains can have independent source activity. Each cluster requires an independent clock, and the CCI requires a clock. "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products
	 **Figure 2-10 CoreTile Express A15×2 A7×3 daughterboard clocks** ARM® CoreTile Express A15×2 A7×3 Technical Reference Manual, available at https://developer.arm.com/documentation/ddi0503/i/

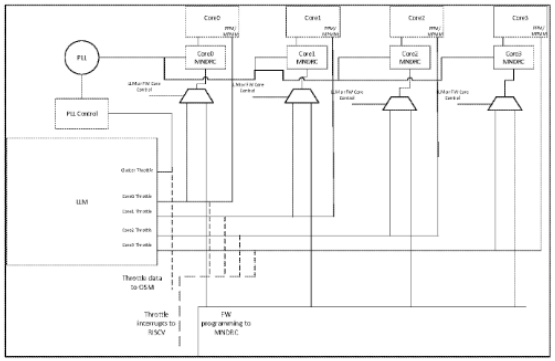
Claim 1	Accused Products
	Qualcomm's documentation demonstrates that the accused devices are configured to contain a first and second set of processor cores according to the above referenced architectures. For example, both the Snapdragon 8 Gen 2 Octa-Core, die code Kailua, and Snapdragon 835 Mobile Platform, MSM8998, are configured with a first set of "Gold" cores and a second set of "Silver" cores, each set having its own PLL Gold or PLL Silver with its own input and output clock signal, and each having a separate power domain and power rails, both the power and output clock signal being variable and the clusters being configured to receive the same: Motivation Current implementation • Current implementation in CPUSS requires that each core per cluster domain run at the same clock frequency. • This requirement is due to the fact that each core doesn't have its own PLL. • OSM aggregates and chooses MAX frequency for operation for those cores. 

Claim 1	Accused Products
	 Kailua

Claim 1	Accused Products

LLM & FW Interaction

- For Kailua implementation the MNDRC's can either be controlled by FW or by LLM directly but not by both.
- When testing for LLM thermal mitigation data the MUX control is switched to LLM that will drive per core MVAL based on it's LUT table.
- When gathering power profile data for SW the MUX control is switched to FW.
- Note that if there is a need to capture data from SW and LLM driven MVAL's to MNDRC then Interrupt driven control is to be used to ensure we have single master that drives MVAL.
- Note that POR implementation for inner and outer loop and per core MPMM/PPM control remains the same.
- The Design has been introduced such that it does not affect POR requirements of LLM and FW



Source sample text

15

Claim 1	Accused Products

Post Waipio Options: Big and Little RISC-V Split(Azzedine)

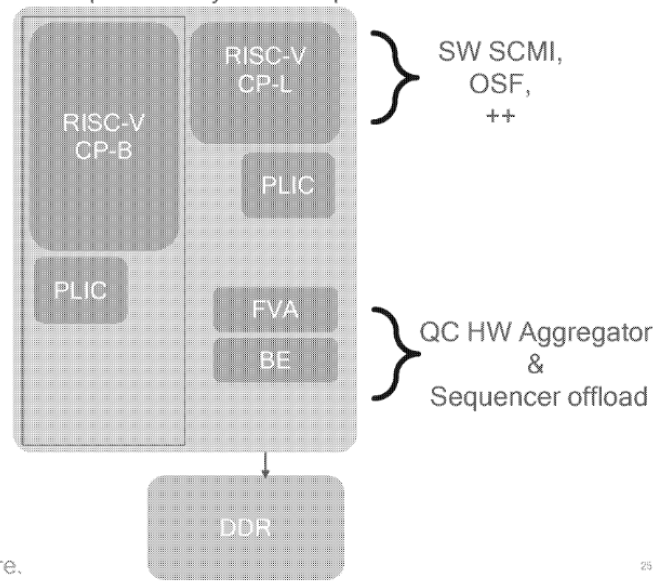
Two RISC-Vs :

1. CP-B: High Frequency (Periodic usage - New features to generate data for CP-L of CPU)
2. CP-L: Low Frequency mode
3. Complex features in "Big" RISC-V (CP-B) will not be propagated to VT
4. Big Risc-V is to be designed in a way that is not be product gating
5. Upgrade to SiFive solution is recommended (to leverage opensource SW tools*.)

SW recommendation for premium for experimentation

*Pulp is not fully compliant to the RISC-V architecture.

Asynchronous
Big Risc-V run periodically waken-up with timer



25

QCREDSTONE_0098870 at -74, -83, -84, -96.

GOLD cluster frequency plan

Mode	PoR Frequency (MHz)	Source (HF PLL)	PLL config							
			VCO freq (MHz)	PLL mode	L Value	PLL div	PLL Power (mW)	Period Jitter (ps)	Half-Cyc jitter (ps)	src_sel
Turbo_L5 CN 0.960V TT/0.960V, SS/xxV	2764	APC1 PLL -early	2764.8	HF	144	1		8.9	23.2	src5
Turbo_L5 0.960V TT/0.960V, SS/xxV	2361	APC1 PLL -early	2361.6	HF	123	1		10.2	26.5	src5
Turbo_L3 CW 0.890V TT/0.890V, SS/0.950V	2361	APC1 PLL -early	2361.6	HF	123	1		10.6	27.5	src5
Turbo_L3 RCW 0.890V TT/0.890V, SS/0.950V	2361	APC1 PLL -early	2361.6	HF	123	1		10.6	27.5	src5

Claim 1	Accused Products

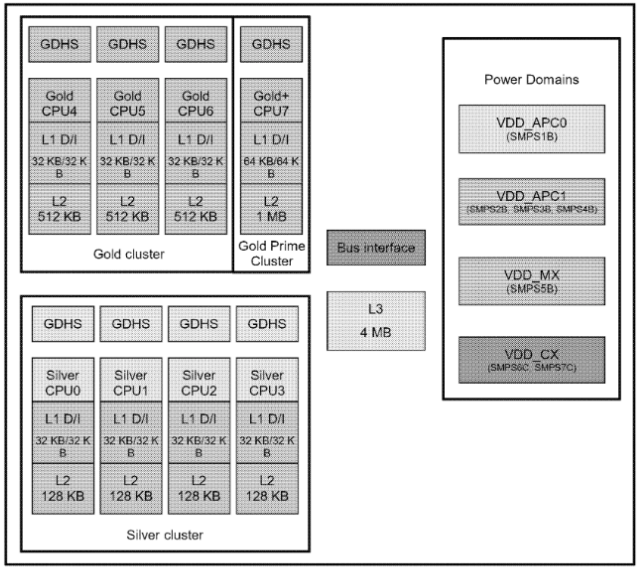
SILVER cluster frequency plan

Mode	PoR Frequency (MHz)	Source (SR PLL)	PLL config							
			VCO freq (MHz)	PLL mode	L Value	PLL div	PLL Power (mW)	Period Jitter (ps)	Half-Cyc jitter (ps)	src_sel
Turbo_L5 CN 0.960V TT/0.960V, SS/xxV	2054	APC0 PLL -early	2054.4	HF	107	1		12.2	31.6	src5
Turbo_L5 0.960V TT/0.960V, SS/xxV	1843	APC0 PLL -early	1843.2	HF	96	1		13.6	35.3	src5
Turbo_L3 CW 0.890V TT/0.890V, SS/0.950V	1843	APC0 PLL -early	1843.2	HF	96	1		13.6	35.3	src5
Turbo_L3 RCW 0.890V TT/0.890V, SS/0.950V	1843	APC0 PLL -early	1843.2	HF	96	1		13.6	35.3	src5
Turbo_L3 CNOM 0.890V TT/0.890V, SS/0.950V	2054	APC0 PLL -early	2054.4	HF	107	1		12.2	31.6	src5
Turbo_L3 0.890V TT/0.890V, SS/0.950V	1843	APC0 PLL -early	1843.2	HF	96	1		13.6	35.3	src5
Turbo_L2 0.800V TT/0.800V, SS/0.860V	1843	APC0 PLL -early	1843.2	HF	96	1		12.2	31.6	src5

QCREDSTONE_0123173 at -73, -77.

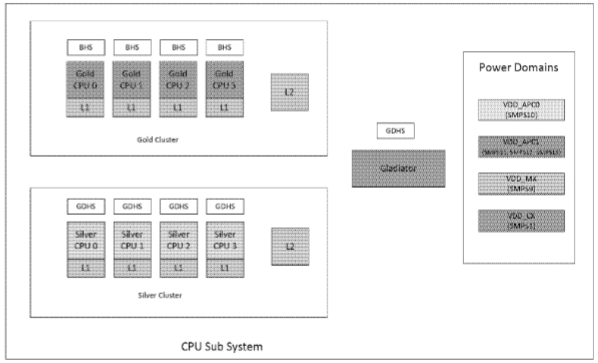
CPUSS

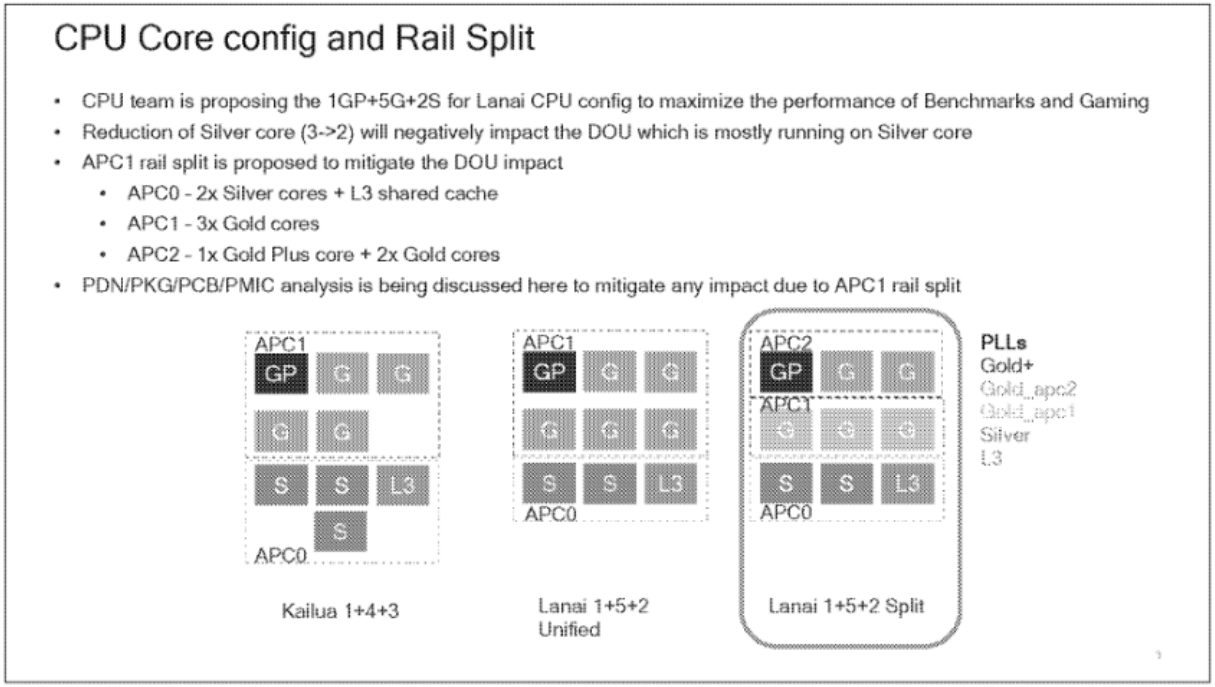
- Kryo 685 Next Gen V8
- Kryo Gold Prime Fmax: 2.6+ GHz
- Kryo Gold Fmax: 2.3+ GHz
- Kryo Silver Fmax: 1.8 GHz
- Kryo Gold Prime L1/L2 cache: 64 KB/1 MB
- Kryo Gold L1/L2 cache: 32 KB/512 KB
- Kryo Silver L1/L2 cache: 32 KB/128 KB
- Frequency of Operation
  - Gold Prime, Gold, Silver, and L3 cache can operate at different frequencies (Independently controlled).
  - Within Silver cluster, all 4 Silver cores and L2 are synchronous.
  - Within Gold cluster, all 3 Gold cores and L2 are synchronous.
  - Within Gold Prime cluster, Gold Prime core and L2 are synchronous
- Power rail
  - Gold Prime core and Gold core share VDD_APC1.
  - Silver core and L3 logic share VDD_APC0.
  - L1 and L2 cache memory cell powered by VDD_MX.
  - Each Kryo Silver/Gold/Gold Prime core has a global distributed head switch (GDHS) to power the core.

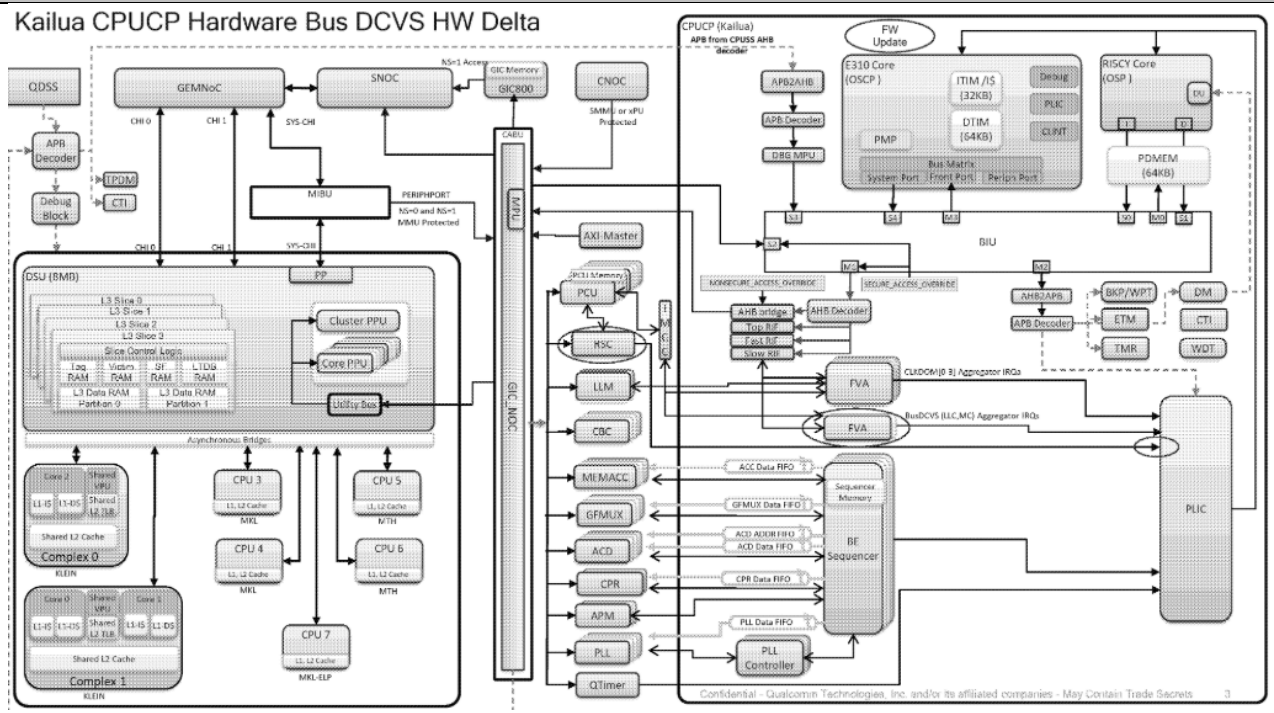


PAGE 10 80-PK177-36 Rev. B July 2020 Confidential – Qualcomm Technologies, Inc. and/or its affiliated companies – May Contain Trade Secrets | MAY CONTAIN U.S. AND INTERNATIONAL EXPORT CONTROLLED INFORMATION

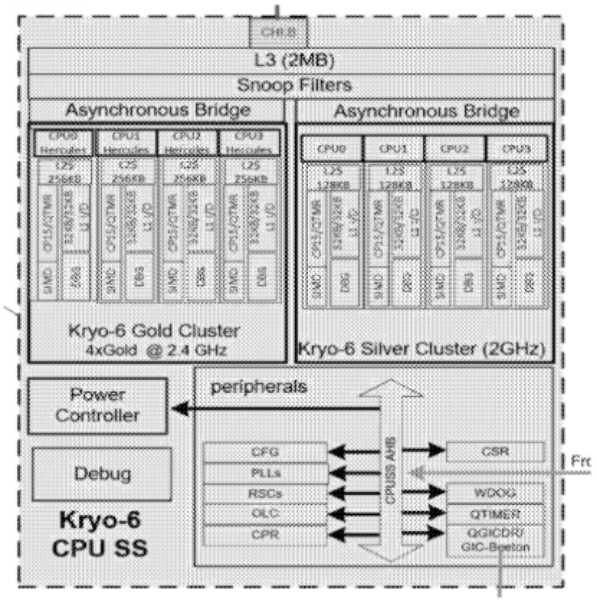
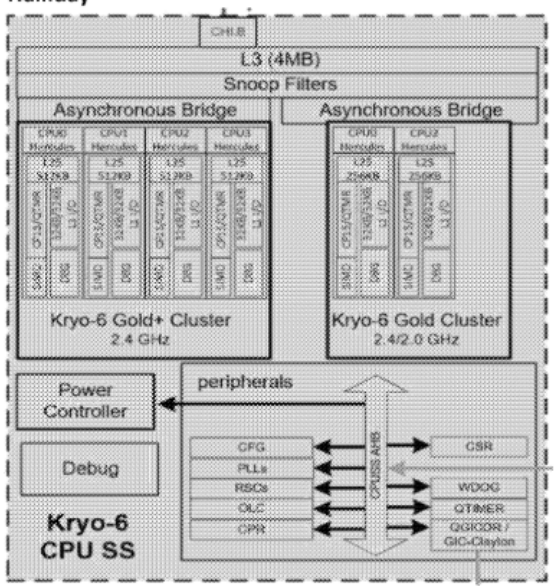
QCREDSTONE_0039762 at -71

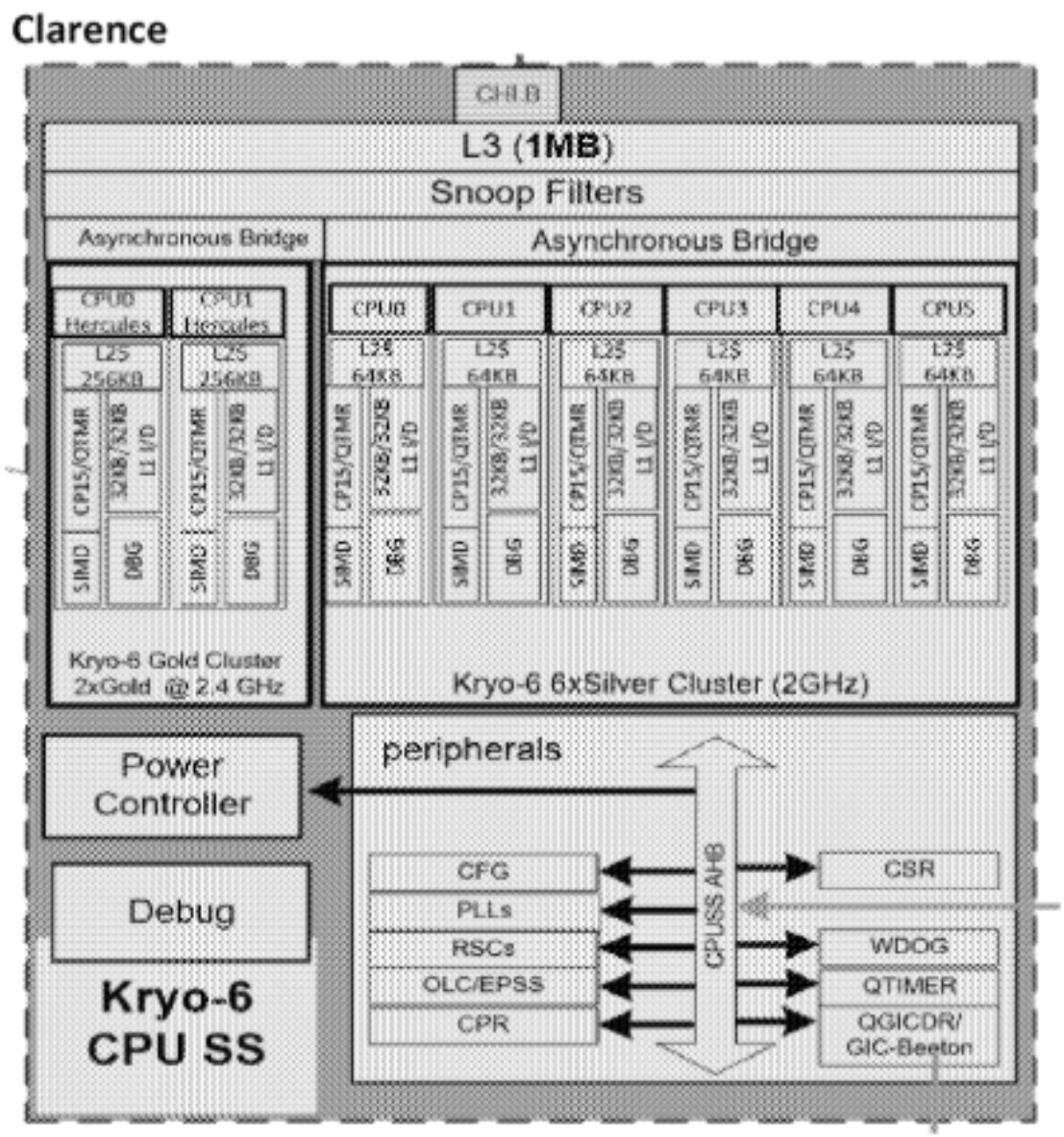
Claim 1	Accused Products
	CPU Power ▪ Customized 64-bit ARM v8-compliant apps processor (Kryo 2xx CPU) ▪ Two Clusters in CPU subsystem – Kryo Gold and Kryo Silver ▪ Kryo Gold Cluster – Quad Kryo high performance CPUs with 2.5 GHz to 2.7 GHz Speed ▪ Kryo Silver Cluster – Quad Kryo low power CPUs with 1.5 GHz to 1.9 GHz Speed ▪ L1 and L2 Cache: ▪ L2 cache at 2 MB for Kryo Gold ▪ L2 cache at 1 MB for Kryo Silver ▪ Power rails: ▪ Kryo Gold cluster and Silver cluster have dedicated, separate power rails ▪ PM8998 SMPS10 powers the Kryo Silver cluster ▪ PM8998 SMPS11/12/13 are tied together as a single trace to power the Kryo Gold cluster ▪ Each Kryo Gold core has a block head switch (BHS) and each Kryo Silver core has a global distributed head switch (GDHS) to power the core ▪ Gold and Silver cluster, along with the respective L2 cache, can operate on a different clock source at different frequencies. ▪ Within a cluster, the cores and L2 are synchronous  QCREDSTONE_0082868 at -878.

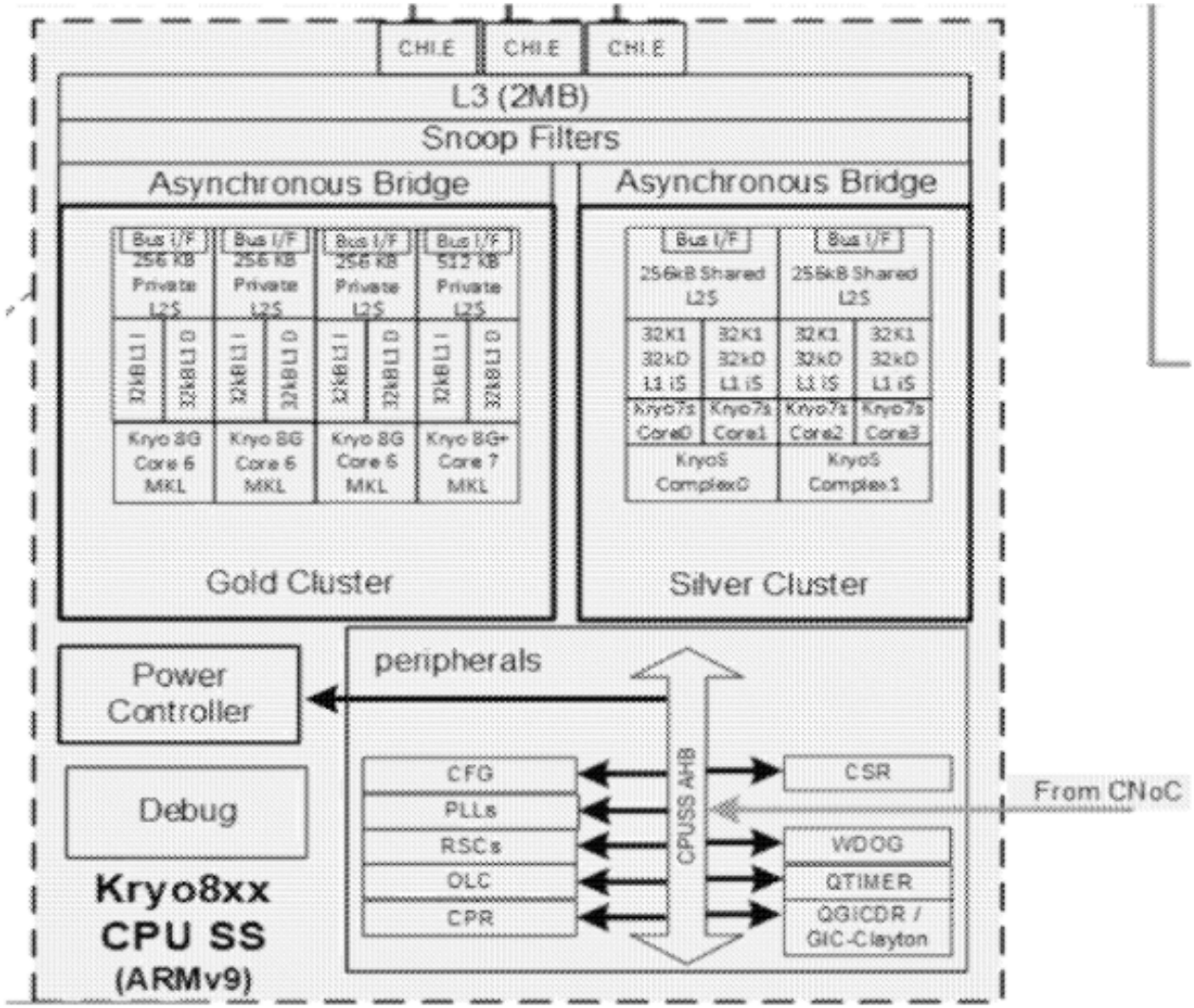
Claim 1	Accused Products
	 QCREDSTONE_0091042 at -44.

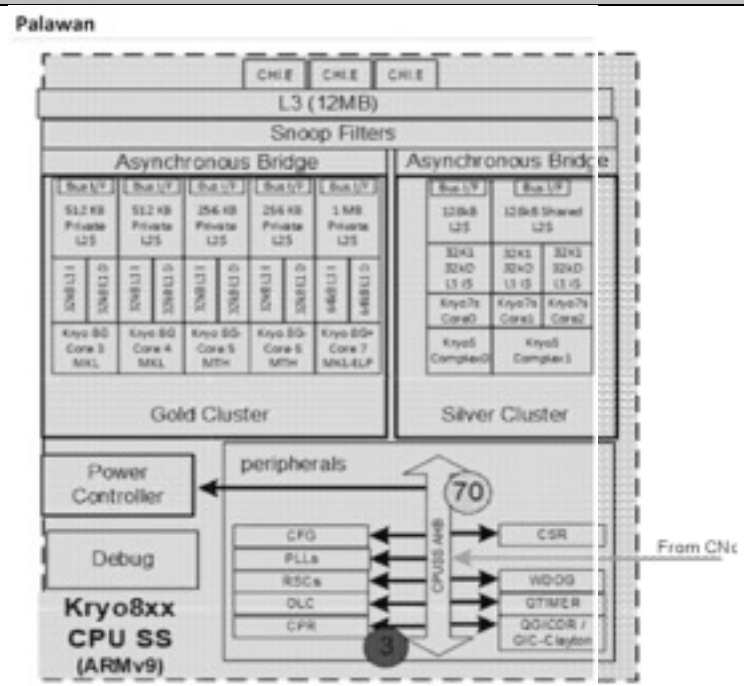
Claim 1	Accused Products
	 QCREDSTONE_0098768 at -70. This arrangement of Gold+, Gold, and/or Silver cores arranged into clusters according to the above referenced architectures is repeated throughout the accused products[1]:

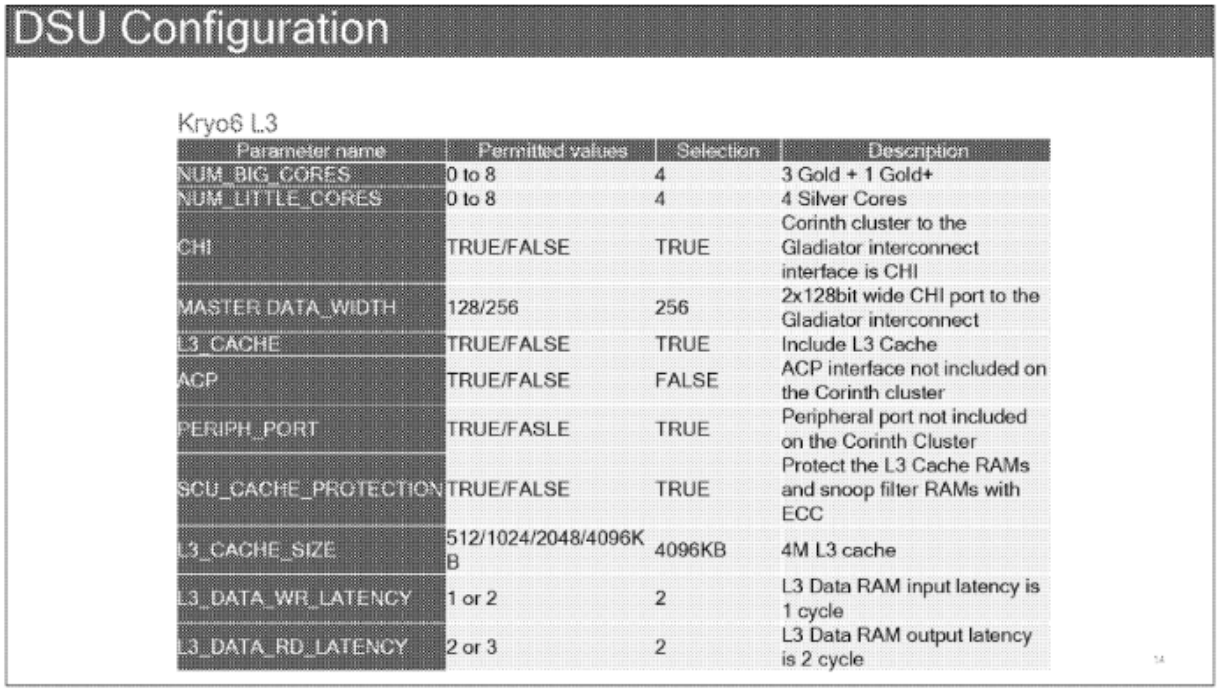
[1] Qualcomm has failed to produce similar diagrams for all accused products/dies or even identified all relevant dies, however the cited documentation demonstrates a common infringing design across all accused products.

Claim 1	Accused Products
	Netrani  Halliday 


Clarence
CHI B
L3 (1MB)
Snoop Filters
Asynchronous Bridge
Asynchronous Bridge
CPU0 Hercules
CPU1 Hercules
L2$ 256KB
CP15/QTIMR
32KB/32KB L1 I/D
SIMD
DBG
CPU0
CPU1
CPU2
CPU3
CPU4
CPU5
L2$ 64KB
Kryo-6 Gold Cluster 2xGold @ 2.4 GHz
Kryo-6 6xSilver Cluster (2GHz)
Power Controller
peripherals
Debug
Kryo-6 CPU SS
CFG
PLLs
RSCs
OLC/EPSS
CPR
CPUSS AHB
CSR
WDOG
QTIMER
QGICDR/ GIC-Beeton

Claim 1	Accused Products
	

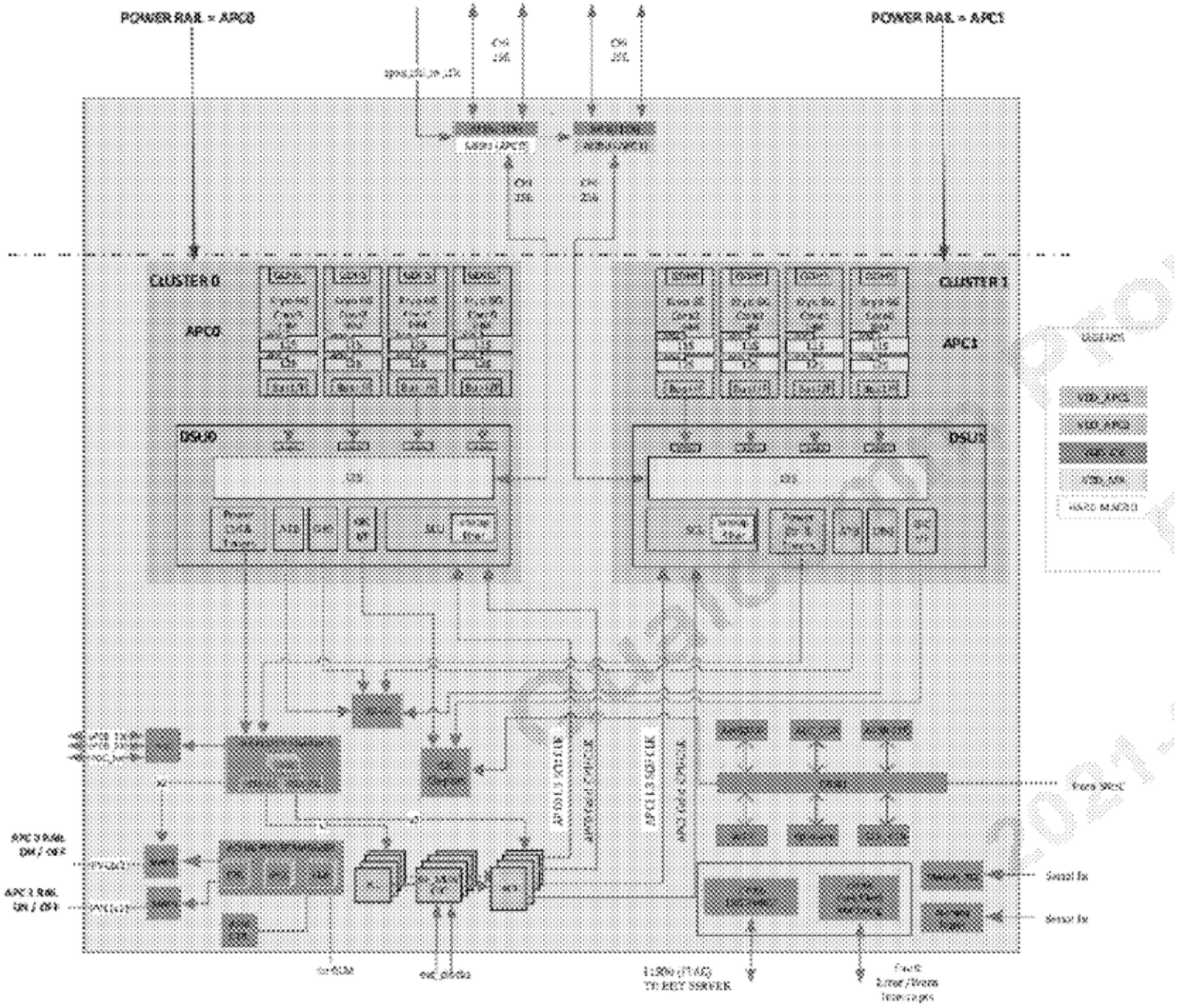
Claim 1	Accused Products
	 QCREDSTONE_0098556 at -558 to -562.

Claim 1	Accused Products
	 QCREDSTONE_0090058 at -71.

DSU Configuration

Kryo6 L3

Parameter name	Permitted values	Selection	Description
NUM_BIG_CORES	0 to 8	4	3 Gold + 1 Gold+
NUM_LITTLE_CORES	0 to 8	4	4 Silver Cores
CHI	TRUE/FALSE	TRUE	Corinth cluster to the Gladiator interconnect interface is CHI
MASTER DATA_WIDTH	128/256	256	2x128bit wide CHI port to the Gladiator interconnect
L3_CACHE	TRUE/FALSE	TRUE	Include L3 Cache
ACP	TRUE/FALSE	FALSE	ACP interface not included on the Corinth cluster
PERIPH_PORT	TRUE/FASLE	TRUE	Peripheral port not included on the Corinth Cluster
SCU_CACHE_PROTECTION	TRUE/FALSE	TRUE	Protect the L3 Cache RAMs and snoop filter RAMs with ECC
L3_CACHE_SIZE	512/1024/2048/4096KB	4096KB	4M L3 cache
L3_DATA_WR_LATENCY	1 or 2	2	L3 Data RAM input latency is 1 cycle
L3_DATA_RD_LATENCY	2 or 3	2	L3 Data RAM output latency is 2 cycle

Claim 1	Accused Products
	

Claim 1	Accused Products

Design Details (Requirements/Features)

CPU

- Dual DSU Octa core processing unit - Le Mans Change
- DSU0 : 4 Kryo6G_prime (Hercules Prime) - Le Mans Change
  - Boot processor
  - 32KB/32KB L1 Cache
  - 256KB L2 Cache
  - APC0 rail
- DSU1 : 4 Kryo6G_prime (Hercules Prime) – Le Mans Change
  - 32KB/32KB L1 Cache
  - 256kB L2 Cache
  - APC1 rail

L3 (Corinth DSU)

- 4MB L3 Cache (2MB per DSU)
  - Async to all CPUs within DSU
  - APC0 rail for DSU0 & APC1 rail for DSU1 – Le Mans Change
  - Full power down mode to reduce power
  - Natively supports dual 256b CHI

Bus Interface

- 2x256b CHI interfaces to GEMNoC from each DSU - Le Mans Change
- I/O Coherency support via CHI
- DVM broadcast to system via CHI
- 64-bit ACE5-Lite Master port interface to system NOC - Le Mans Change
- 32-bit AHB Slave port interface to system NOC
- 32-bit AHB Master port interface to system NOC (EPSS)
- APB Slave port interface to system DAP
- ATB bus interface to CoreSight Trace component
- Time Stamp interface to CoreSight debug component
- TAP port interface to JTAG interface

AUTO

- Fault Monitoring for Safety Manager.
- LBIST and MBIST Capability at Cold Boot.
- IEEE1500 Interface for LBIST Infrastructure from SoC.
- Error And Parity Checks.
- Clock Monitoring.
- 2D parity for CSRs (excluding ARM logic CSRs) - Le Mans Change

Power

- OSM3.1 – EPSS for Active Power Management
- Low power modes for aggressive dynamic & leakage mitigation.
- MPMM Support by Hercules ARM Cores.
- EPSS access to DDR via AHB (Use cases: self-loading single image of EPSS, Schedule assistance by providing shared data, Error recovery implementation, ARM SCP (SCMI based) prototype)

Qualcomm Proprietary Confidential

Claim 1	Accused Products

3rd Party

Third Party IPs (3PIP) and Export Controlled IP

Do you have any 3rd Party IPs to declare? (note that this is a sign-off on the accuracy of your answer, which may have financial implications):
YES

Supplier	Licensed IP Description	# Instances	Changed from Previous Program (Y/N)?	QCOM Owner	Delta Comments
Arm Limited	Hercules Processor/Hercules Crypto/HerculesPrime Processor/HerculesPrime Crypto/Dynamiq Shared Unit 8MB Version (DSU 8MB)	8	yes		L1/L2 size changed from 64KB/512KB to 32KB/256KB
Arm Limited	Hercules Processor/Hercules Crypto/HerculesPrime Processor/HerculesPrime Crypto/Dynamiq Shared Unit 8MB Version (DSU 8MB)	2	yes		L3 size changed from 8MB to 2MB (per cluster)
Arm Limited	GIC-Clayton Generic Interrupt Controller	1	yes		GIC Beeton is replaced with GIC Clayton
Arm Limited	Coresight Components-Various	1	no		
PULP Platform	RI5CY RISC-V Core (Open Source Hardware Platform) https://www.pulp-platform.org/	1	no		

QCREDSTONE_0091177 at -86-87, -248.

GOLD_PLUS frequency plan										
Mode	PoR Frequency (MHz)	Source (HF PLL)	PLL config							
			VCO freq (MHz)	PLL mode	L Value	PLL div	PLL Power (mW)	Period Jitter (ps)	Half-Cyc jitter (ps)	src_sel
Turbo_L5 CN 0.960V TT/0.960V, SS/xxV	2956	APC1 PLL -early	2956.8	HF	154	1		8.5	22.0	src5
Turbo_L5 0.960V TT/0.960V, SS/xxV	2572	APC1 PLL -early	2572.8	HF	134	1		10.0	26.0	src5
Turbo_L3 CW 0.890V TT/0.890V, SS/0.950V	2457	APC1 PLL -early	2457.6	HF	128	1		10.3	26.7	src5

GOLD cluster frequency plan										
Mode	PoR Frequency (MHz)	Source (HF PLL)	PLL config							
			VCO freq (MHz)	PLL mode	L Value	PLL div	PLL Power (mW)	Period Jitter (ps)	Half-Cyc jitter (ps)	src_sel
Turbo_L5 CN 0.960V TT/0.960V, SS/xxV	2764	APC1 PLL -early	2764.8	HF	144	1		8.9	23.2	src5
Turbo_L5 0.960V TT/0.960V, SS/xxV	2361	APC1 PLL -early	2361.6	HF	123	1		10.2	26.5	src5

Claim 1	Accused Products

SILVER cluster frequency plan

Mode	PoR Frequency (MHz)	Source (SR PLL)	PLL config							
			VCO freq (MHz)	PLL mode	L Value	PLL div	PLL Power (mW)	Period Jitter (ps)	Half-Cyc jitter (ps)	src_sel
Turbo_L5 CN 0.960V TT/0.960V, SS/xxV	2054	APC0 PLL -early	2054.4	HF	107	1		12.2	31.6	src5
Turbo_L5 0.960V TT/0.960V, SS/xxV	1843	APC0 PLL -early	1843.2	HF	96	1		13.6	35.3	src5
Turbo_L3 CW 0.890V TT/0.890V, SS/0.950V	1843	APC0 PLL -early	1843.2	HF	96	1		13.6	35.3	src5

PLL						
	APSS_CC_SILVER_PLL	apss_cc_silver_pll	1344.00	PLL_SILVER_NOM	1	1478.40
	APSS_CC_SILVER_PLL_EARLY_GRP	apss_cc_silver_pll_out_main	1344.00	PLL_SILVER_NOM	1	1478.40
	APSS_CC_SILVER_PLL_MAIN_GRP	apss_cc_silver_pll_out_even	1344.00	PLL_SILVER_NOM	1	1478.40
	APSS_CC_SILVER_PLL_TEST_GRP	apss_cc_silver_pll_out_test	1344.00	PLL_SILVER_NOM	1	1478.40
	APSS_CC_GOLD_PLL	apss_cc_gold_pll	1401.60	PLL_GOLD_NOM	1	1593.60
	APSS_CC_GOLD_PLL_EARLY_GRP	apss_cc_gold_pll_out_main	1401.60	PLL_GOLD_NOM	1	1593.60
	APSS_CC_GOLD_PLL_MAIN_GRP	apss_cc_gold_pll_out_even	1401.60	PLL_GOLD_NOM	1	1593.60
	APSS_CC_GOLD_PLL_TEST_GRP	apss_cc_gold_pll_out_test	1401.60	PLL_GOLD_NOM	1	1593.60
	APSS_CC_L3_PLL	apss_cc_l3_pll	1209.60	PLL_L3_NOM	1	1344.00
	APSS_CC_L3_PLL_EARLY_GRP	apss_cc_l3_pll_out_main	1209.60	PLL_L3_NOM	1	1344.00
	APSS_CC_L3_PLL_MAIN_GRP	apss_cc_l3_pll_out_even	1209.60	PLL_L3_NOM	1	1344.00
	APSS_CC_L3_PLL_TEST_GRP	apss_cc_l3_pll_out_test	1209.60	PLL_L3_NOM	1	1344.00
	APSS_CC_GOLD_PLUS_PLL	apss_cc_gold_plus_pll	1459.20	PLL_GOLD_PLUS_NOM	1	1651.20
	APSS_CC_GOLD_PLUS_PLL_EARLY_GRP	apss_cc_gold_plus_pll_out_main	1459.20	PLL_GOLD_PLUS_NOM	1	1651.20
	APSS_CC_GOLD_PLUS_PLL_MAIN_GRP	apss_cc_gold_plus_pll_out_even	1459.20	PLL_GOLD_PLUS_NOM	1	1651.20
	APSS_CC_GOLD_PLUS_PLL_TEST_GRP	apss_cc_gold_plus_pll_out_test	1459.20	PLL_GOLD_PLUS_NOM	1	1651.20

Claim 1	Accused Products

Clock Source Data	PLL Fractional or Integer Multiplication				Source Period	Duty Cycle
Root Clock Src	PLL L	PLL M	PLL N	Frequency (MHz)	Jitter (ns)	Jitter (ns)
Tester				40.00	0.500	0.500
XO				19.20	0.500	0.500
SLEEP_CLK				0.03	0.500	0.500
PLL_GOLD_CW	123	0	1	2361.60	0.0106	0.0275
PLL_GOLD_RCW	123	0	1	2361.60	0.0106	0.0275
PLL_GOLD_CNOM	141	0	1	2707.20	0.0092	0.0240
PLL_GOLD_TURBO_L1	108	0	1	2073.60	0.0121	0.0314
PLL_GOLD_TURBO_L0	95	0	1	1824.00	0.0137	0.0356
PLL_GOLD_NOM_L1	83	0	1	1593.60	0.0155	0.0403
PLL_GOLD_NOM	73	0	1	1401.60	0.0178	0.0464
PLL_GOLD_SVS_L1	62	0	1	1190.40	0.0210	0.0630
PLL_GOLD_SVS	49	0	1	940.80	0.0372	0.0798
PLL_GOLD_SVS2	33	0	1	633.60	0.0711	0.1343
PLL_GOLD_SVS3	6	0	1	115.20	0.0883	0.1488
PLL_SILVER_CW	96	0	1	1843.20	0.0136	0.0353
PLL_SILVER_RCW	96	0	1	1843.20	0.0136	0.0353
PLL_SILVER_CNOM	107	0	1	2054.40	0.0122	0.0316
PLL_SILVER_TURBO_L1	96	0	1	1843.20	0.0136	0.0353
PLL_SILVER_TURBO_L0	89	0	1	1708.80	0.0146	0.0381
PLL_SILVER_NOM_L1	77	0	1	1478.40	0.0167	0.0434
PLL_SILVER_NOM	70	0	1	1344.00	0.0186	0.0484
PLL_SILVER_SVS_L1	58	0	1	1113.60	0.0227	0.0587
PLL_SILVER_SVS	47	0	1	902.40	0.0388	0.0831
PLL_SILVER_SVS2	31	0	1	595.20	0.0341	0.0341
PLL_SILVER_SVS3	6	0	1	115.20	0.0883	0.1488
PLL_L3_CW	83	0	1	1593.60	0.0157	0.0408
PLL_L3_RCW	83	0	1	1593.60	0.0157	0.0408
PLL_L3_CNOM	94	0	1	1804.80	0.0139	0.0360
PLL_L3_TURBO_L1	83	0	1	1593.60	0.0157	0.0408
PLL_L3_TURBO_L0	78	0	1	1497.60	0.0167	0.0434
PLL_L3_NOM_L1	70	0	1	1344.00	0.0186	0.0484
PLL_L3_NOM	63	0	1	1209.60	0.0207	0.0538
PLL_L3_SVS_L1	52	0	1	998.40	0.0351	0.0744
PLL_L3_SVS	42	0	1	806.40	0.0437	0.0933
PLL_L3_SVS2	27	0	1	518.40	0.0549	0.0549
PLL_L3_SVS3	6	0	1	115.20	0.0883	0.1488
PLL_GOLD_TEST	54	0	1	2073.60	0.0121	0.0314
PLL_SILVER_TEST	54	0	1	1843.20	0.0136	0.0353

QCREDSTONE_0123173 at -173 to -177, -183, -316. *See also* QCREDSTONE_0108055, QCREDSTONE_010943, QCREDSTONE_0110523, QCREDSTONE_0112461, QCREDSTONE_0113841, QCREDSTONE_0114427, QCREDSTONE_0115813, QCREDSTONE_0116536, QCREDSTONE_0117594; QCREDSTONE_0120263, QCREDSTONE_0124233, QCREDSTONE_0125186, QCREDSTONE_0131099.

Claim 1	Accused Products

Power Model

PEU

- Dynamic power model:
  - Pdyn = α * IPC * V^2 * f
  - Alpha value is tuned per corner (LowSVS, SVS, …, Nominal, …, Turbo)
    - GoldPlus and Gold: 9 alpha values each
    - Silver: 6 alpha values

Power Model

PEU

- Registers:
  - **Voltage:** APSS_SILVER_CPRh_STATUS_[0-1] / APSS_GOLD_CPRh_STATUS_[0-1]
    - DCVSh_corner_last_voltage
  - **Frequency:** EPSSSLOW_CLKDOM[0/1/2/3]_DOMAIN_STATE
    - LVAL
  - **Temperature:** APSS_SILVER_LMH_LLM_TEMP_RX_STS_0_i / APSS_GOLD_LMH_LLM_TEMP_RX_STS_0_i
  - **IPC:** PMU registers - Instructions and cycles (PMEVCNTR0_EL0, PMCCNTR_EL0)

QCREDSTONE_0099078 at -82 to -83.

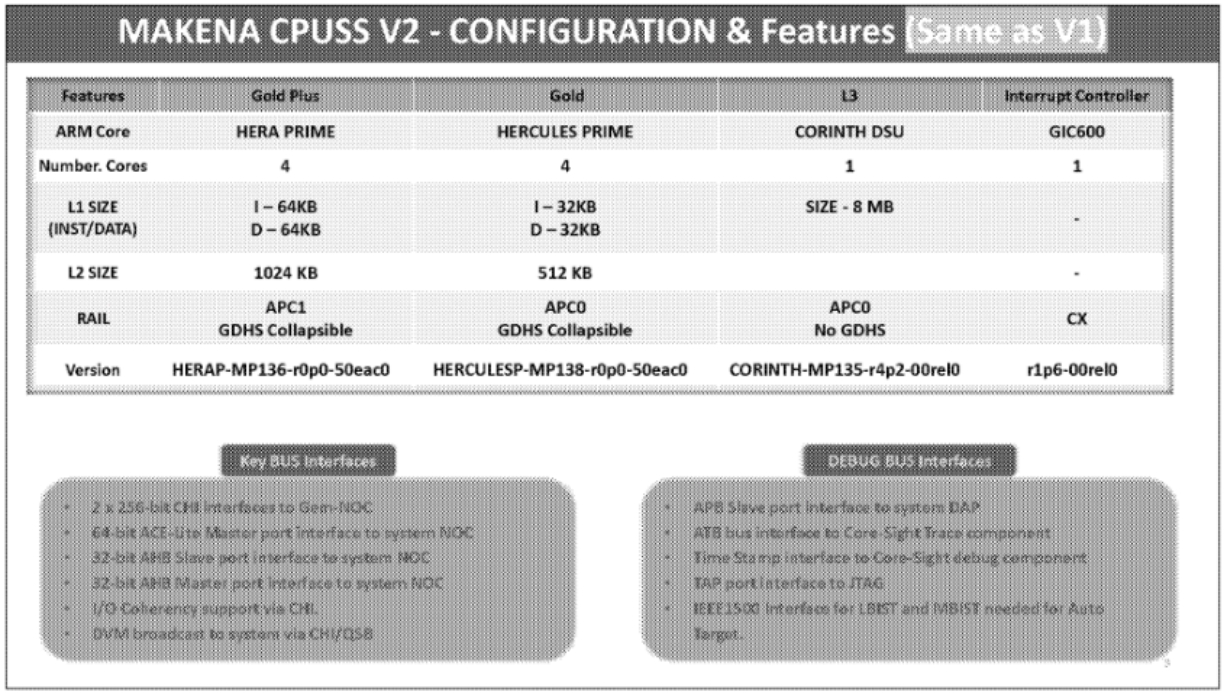
Claim 1	Accused Products

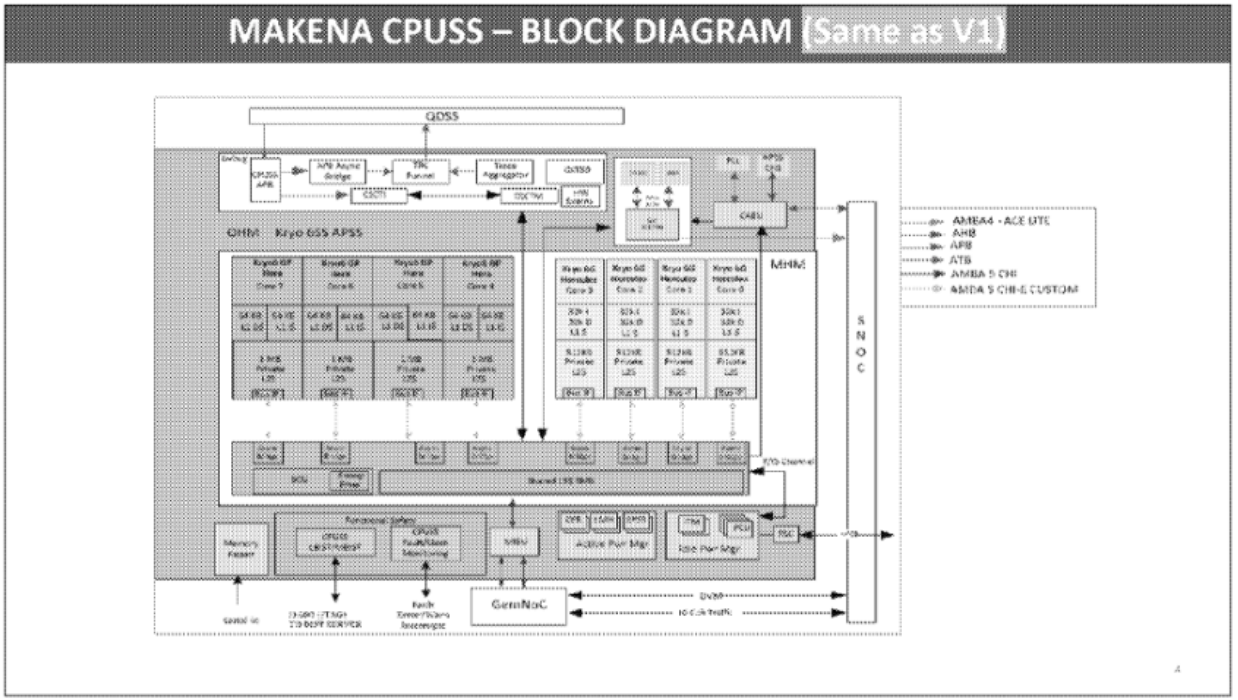
Lanai R2 pre-silicon performance validation

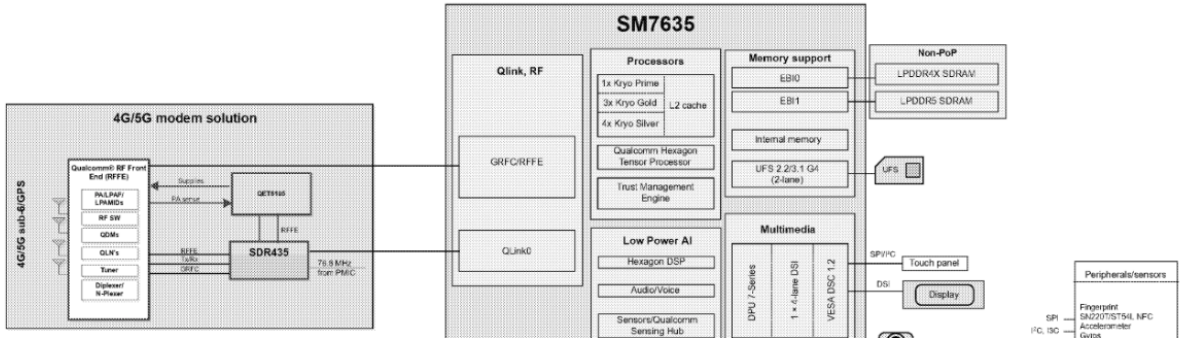
Configuration

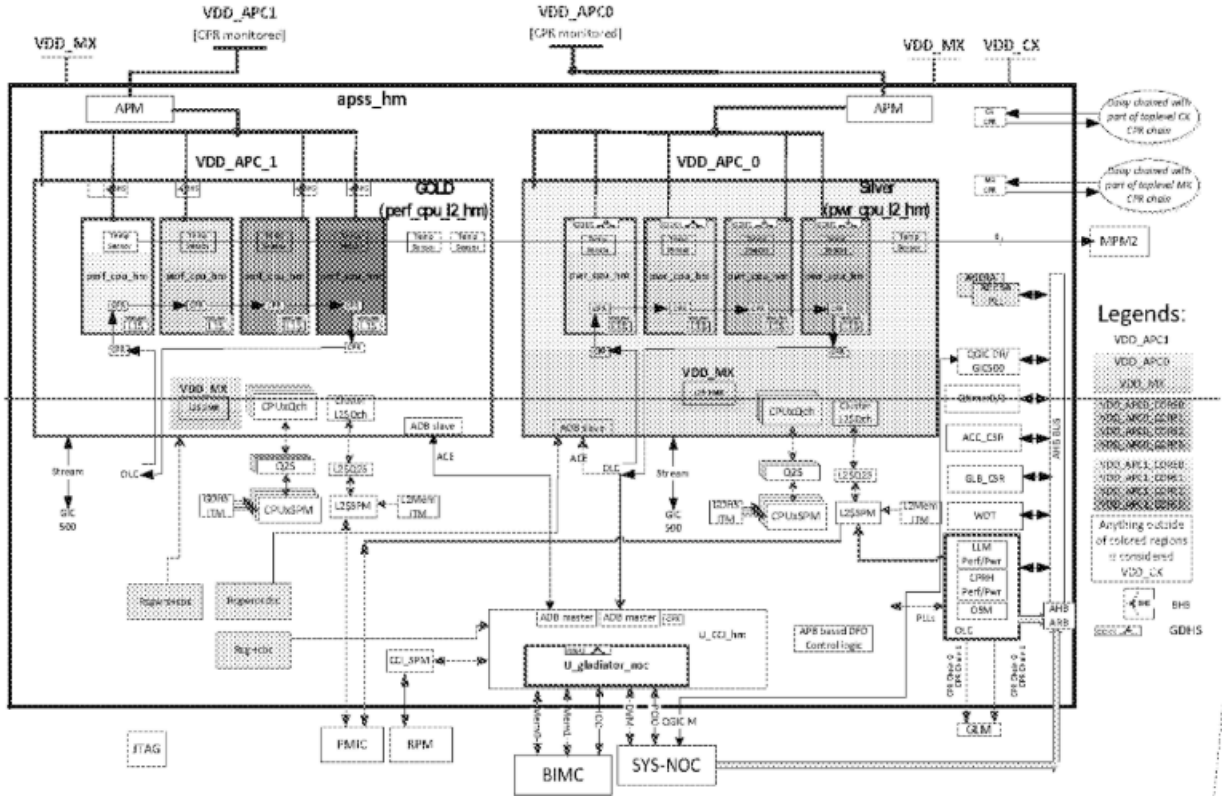
Chipset	Kailua R2 RUMI Pre-silicon [illegible]	Lanai V1 RUMI Pre-silicon [illegible]	Lanai R2 RUMI Pre-silicon [illegible]
GOLD+ Frequency (MHz)	1xMKL-ELP@2838.9	1xHUNTER-ELP@2885.1	1xHUNTER-ELP@2885.1
GOLD Frequency (MHz)	2xMKL/2xMTH@2620.7	5xHUNTER@2589.2	5xHUNTER@2589.2
SILVER Frequency (MHz)	3xKlein@2197.9	2xHayes@2148.5	2xHayes@2148.5
L3 Frequency (MHz)	1892.7	1905.3	1905.3
LLC Frequency (MHz)	1064.6	1062.9	1062.9
DDR Frequency (MHz)	4260.2	4207.8	4207.8
Gold +: Cache Size [L2/L1i/L1d] KB	1024/64/64	2048/64/64	2048/64/64
Gold (MTH): Cache Size [L2/L1i/L1d] KB	256/32/32	-	-
Gold (MKL/HUNTER): Cache Size [L2/L1i/L1d] KB	512/32/32	512/64/64	512/64/64
Silver(complex): Cache Size [L2/L1i/L1d] KB	128*/32/32	512*/64/64	512*/64/64
Silver(single): Cache Size [L2/L1i/L1d] KB	128/32/32	-	-
L3: Cache Size MB	8	12	12
LLC: Cache Size MB	6(3 for CPU)	8(5 for CPU)	(5 for CPU)
DDRSS	4ch LP5	4ch LP5	4ch LP5
Build	E3.0	E3.5 (RUMI.V1.SOC.EPSILON4_LPDDR5_GPU)	RUMI.R2.SOC.ALPHA1_LPDDR5
Convex version	convex_2021_08_20_ver_03_09	convex_2022_06_16_ver_03.14	r2_convex_sandbox(early stage)

QCREDSTONE_0090953 at -84.

Claim 1	Accused Products
	

Claim 1	Accused Products
	 QCREDSTONE_0092294 at -96, -97.

Claim 1	Accused Products
	1.1 Functional block diagram  **1.2 SM7635 features** **NOTE** Some of the hardware features integrated within the SM7635 must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SM7635 features. **Table 1-1 SM7635 features** **Feature** / **SM7635 capability** ***Processors*** Applications ▪ Kryo CPU 7-Series built on Arm Cortex technology ▫ Kryo Prime: One high-performance core ▫ Kryo Gold: Three high-performance cores ▫ Kryo Silver: Four low-power cores QCREDSTONE_0013455 At -64, -65.

Claim 1	Accused Products
	 QCREDSTONE_0096091 at -104.
[1b] a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply	Each Accused Product comprises a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal. For example, in addition to the first set of processor cores, the Snapdragon 8 Gen 2 Octa-Core has a second set of high-performance processor cores (two or more ARM Cortex-A710 cores). For

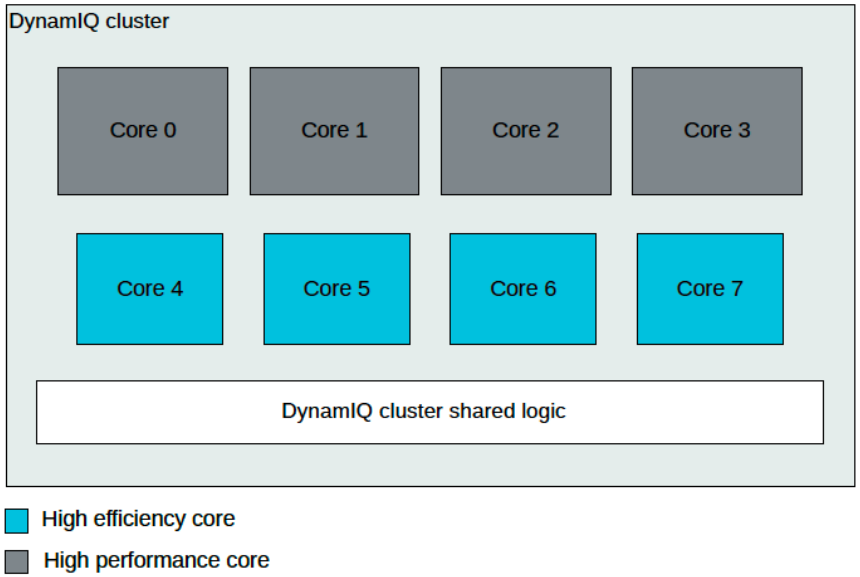
Claim 1	Accused Products
voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and	another example, in addition to the first set of processor cores, the Snapdragon 8 Gen 2 Octa-Core has a second set of high-performance processor cores (two or more ARM Cortex-A715 cores). The processor cores in the second set receive a second, independent dynamic supply voltage and a second clock signal of a second PLL receiving an independent second clock signal. For a further example, in addition to the first set of processor cores, the Snapdragon 835 Mobile Platform has a second set of high-performance processor cores (two or more A73 cores). The processor cores in the second set receive a second, independent dynamic supply voltage and a second clock signal of a second PLL receiving an independent second clock signal. ARM documentation for the big.LITTLE and DynamIQ architectures used in the Accused Products directly shows that each core cluster receives its own clock domain. At the time the Accused Products were designed, it was typical to produce this clock using a PLL that has a corresponding clock input. Furthermore, ARM documentation for an earlier, related device (the Cortex-A15_A7 MPCore test chip, which also has independent clock domains for different CPU clusters) shows each CPU cluster receiving an output clock signal from a PLL having a corresponding clock signal as input (*e.g.* from an oscillator). *See, e.g.*:

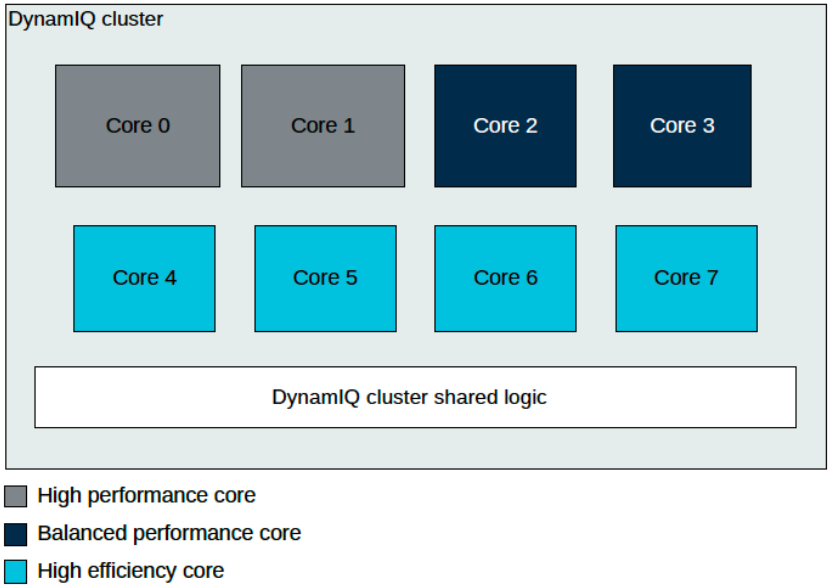
Claim 1	Accused Products

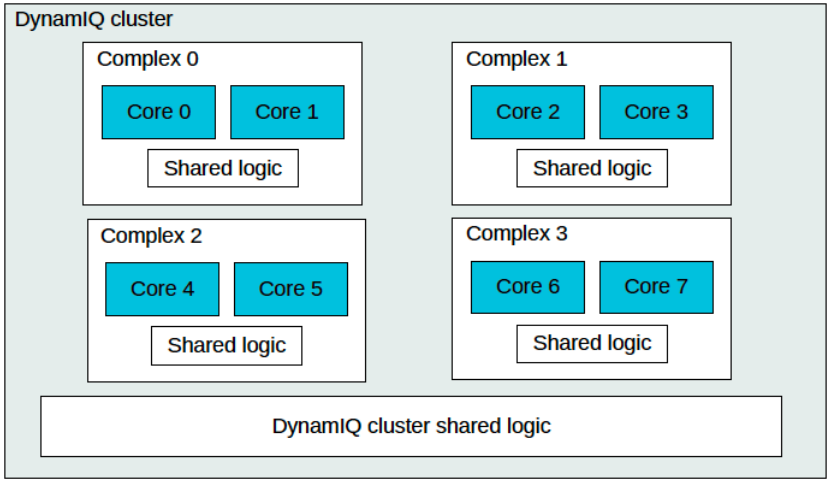
	Snapdragon 8 Gen 2 (2023) [edit]
	The **Snapdragon 8 Gen 2** was announced on November 15, 2022.[252]
	Notable features over its predecessor (8 Gen 1):
	• 4nm (TSMC N4) process
	• Support up to 16 GB LPDDR5X 4200 MHz
	• Support UFS 4.0
	• CPU features
	  • 1 Kryo Prime (ARM Cortex-X3), up to 3.36 GHz. Prime core
	  • 1MB L2 cache
	  • Only 64-bit support [253]
	  • 2 Kryo Gold (ARM Cortex-A715), up to 2.8 GHz. High Performance cores
	  • Only 64-bit support [253]
	  • 2 Kryo Gold (ARM Cortex-A710), up to 2.8 GHz. Performance cores
	  • 32-bit and 64-bit support[253]
	  • 3 Kryo Silver (ARM Cortex-A510), up to 2 GHz. Efficiency cores
	  • 32-bit and 64-bit support[253]
	  • 35% performance uplift and 40% power efficiency improvement
	  • 8 MB system-level cache
	https://en.wikipedia.org/wiki/List_of_Qualcomm_Snapdragon_systems_on_chips#Snapdragon_8_Gen_2_(2023)

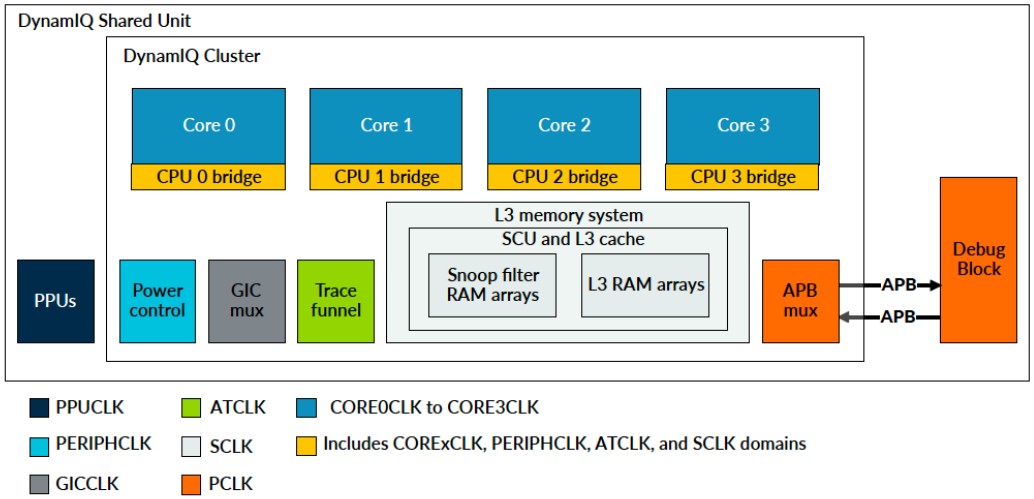
<table>
<tr><th>Claim 1</th><th>Accused Products</th></tr>
<tr><td></td><td>
<table>
<tr><th>Model number</th><th>Product Name</th><th>Fab</th><th>Die size</th><th>CPU</th></tr>
<tr><td>MSM8998[246]</td><td>Snapdragon 835</td><td>10 nm FinFET (Samsung 10LPE)</td><td>72.3 mm^2</td><td>4 + 4 cores Kryo 280 (2.45 GHz Cortex-A73 + 1.9 GHz Cortex-A53)</td></tr>
</table>
https://en.wikipedia.org/wiki/List_of_Qualcomm_Snapdragon_systems_on_chips#Snapdragon_800_series_(2013%E2%80%932021)
</td></tr>
</table>

Claim 1	Accused Products
	Cluster features The DSU-110 has the following cluster features: • Support for Arm®v9.0-A architecture cores • Support for up to four types of core, and a maximum of 12 cores in the cluster • *Power Policy Units* (PPUs) providing autonomous power management of the L3 cache and the cores • Support for cores running independently at different frequencies and voltages known as *Dynamic Voltage Frequency Scaling* (DVFS). For cores in a complex, DVFS is only possible for the whole complex not for individual cores. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual, available at https://documentation-service.arm.com/static/62bb28beb334256d9ea8cc32, at p. 19 A cluster can be configured with up to four different types of cores in the same cluster. Each core type targeting different power efficiency and performance levels. This arrangement allows for an intermediate core that has an intermediate performance and efficiency level. The cluster also supports complexes. A cluster can be configured in many arrangements. Examples of cluster arrangements are: • One or more cores of the same type. • Various arrangements of two types of cores. For example, one or more cores targeting either a high-performance level or a higher power efficiency level. • Various arrangements of three or four types of cores. For example, one or more high-peformance cores, power-efficient cores, and intermediate cores. • One or more complexes and no individual cores. For information on complexes, see 2.3.1 What is a complex? on page 25. • One or more complexes and individual cores. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 22

Claim 1	Accused Products
	 Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 23

Claim 1	Accused Products
	 Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 24

Claim 1	Accused Products
	 Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 24 The DSU-110 DynamIQ™ cluster supports blocks that are called complexes which contain up to two cores of the same type and some shared logic. Sharing some logic between the two cores of a dual core complex can make the dual core complex area efficient. However, this area efficiency is at the cost of reduced performance compared with using two single-core complexes. Arm® DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 25

Claim 1	Accused Products
	The *DynamIQ™ Shared Unit-110* (DSU-110) has multiple clock domains. Each core or complex can be implemented in a separate clock domain. The following figure shows the clock domains for an example cluster with four standalone cores. **Figure 4-1: DSU-110 clock domains**  Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 46

Claim 1	Accused Products
	6.1 The Power Policy Unit Power mode control for the *DynamIQ™ Shared Unit-110* (DSU-110) is provided by the *Power Policy Units* (PPUs) that are integrated into the cluster. These PPUs control all the PPU modes for all components in the cluster. A PPU is a standard component for abstracting software-controlled power domain policy to low-level hardware control signaling. There is one PPU for controlling the DSU-110 DynamIQ™ cluster power domain (PDCLUSTER). Also, each core has its own individual PPU for controlling its respective core power domain (for example, a PPU for PDCORE0 and a PPU for PDCORE1). This includes any cores included as part of a complex. A component in the system such as a *System Control Processor* (SCP) can program the PPUs through the utility bus to set the required power policy. The PPUs control the low-level details of powering up, powering down, and resetting domains as necessary to implement the requested policy. The hardware performs any actions to reach the requested power mode, such as gating clocks, cleaning and invalidating caches, or disabling coherency. Note • Although the cluster and each core in the cluster has their own PPU, the shared logic of a complex does not have a dedicated PPU. Instead, power management of the complex is controlled as a combination of the PPUs for the cores it contains. See Table 5-8: PPU mode and power domain states for a dual-core complex on page 74. • The cluster and all the core PPUs are provided as part of the DSU-110. • The implementation process automatically creates the PPU for the cluster and each core PPU, and connects these into the DSU-110 DynamIQ™ cluster. Each PPU has a set of memory-mapped control registers which is accessed using the utility bus. *Id.* at p. 78

Claim 1	Accused Products

The *DynamIQ™ Shared Unit-110* (DSU-110) *Power Policy Units* (PPUs) control power management for the Cortex®-A510 core. A Cortex®-A510 complex supports separate gated power domains for the complex, for each core inside the complex, and for the *Vector Processing Unit* (VPU). It also supports a dedicated voltage domain for each complex, and a voltage domain for the DSU-110 DynamIQ™ cluster.

Arm Cortex-A510 Core Technical Reference Manual at p. 39

The cluster contains several clock domains for functionality that is likely to be connected to different clocks in the system. Within each core, the CPU bridge contains asynchronous bridges fo all crossings between the core and cluster clock domains. Each CPU bridge is split, with one half of each bridge in the core clock domain and the other half in the relevant cluster domain. At the cluster level, there is the *Snoop Control Unit* (SCU) bridge which contains crossings between the cluster clock domains as required.

Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 46

The DynamIQ Shared Unit-110 (DSU-110) has a separate clock signal for each standalone core or complex. There are also separate clocks for the internal logic, and some of the e interfaces.

The following table describes the clock signals of the DSU-110.

Table 1. DSU-110 clock signals

Signal	Description
COREyCLK	The clocks for each of the cores in the cluster that are not part of a complex. y is the core instance number, for example, CORE0CLK is the clock for core 0. These signals clock all core logic, including L1 and L2 caches.
COMPLEXxCLK	The clocks for each complex in the cluster. Each clock is connected to all cores in the respective complex. x is the complex instance number, for example, COMPLEX0CLK is the clock for complex 0.

https://developer.arm.com/documentation/101381/0400/Clocks-and-resets/Clocks-

Claim 1	Accused Products

4.1.1 Input clocks

Input clocks must be provided with a source that is external to, or embedded in, the subsystem.

Table 4-1: Input clocks

Clock	Description
REFCLK	Main reference clock The input clock to *System Control Processor* (SCP) boots coming out of reset. REFCLK also clocks other logic like SCP generic and watchdog timers.
CPUxPLLCLKn	CPUxPLLCLKn is a high-frequency reference clock inputs used for application core PLL, that is, one per core, where n = 0-7.
CLUS0PLLCLKn	CLUS0PLLCLKn is a high-frequency reference clock inputs used for cluster PLL, that is, one clock per cluster, where n is the number of clusters in a subsystem. As RD-TC21 reference subsystem only contain one cluster, n is fixed to 1.
INTPLLCLK	INTPLLCLK is a high-frequency reference clock input used for the Interconnect block.
SYSPLLCLK	SYSPLLCLK is a high-frequency clock input for the main block.
DMCPLLCLK	DMCPLLCLK is a high-frequency reference clock input used for the Memory block.
GPUPLLCLK	GPUPLLCLK is a high-frequency reference clock input used for the GPU block.

Arm® Total Compute 2021 Reference Design Software Developer Guide at p. 40

4.1.2 Systems clocks

RD-TC21 internally derives clocks that are used for parts of the subsystem. These clocks are generated only when the VSYS.SYSTOP power domain is powered. Each clock can be individually controlled.

The following table summarizes these derived internal clocks.

Id.

Claim 1	Accused Products

Table 4-2: Systems internal derived clocks

Clock Signal	PLL	Description
CLUSxCORECLKn n is the number of clusters in a subsystem.	CPUPLL	Core clock. Each core is clocked independently to each other. Therefore, One clock per cluster, where
CLUSxCLK	CLUSxPLLCLKn	CPU Cluster x clock. The cluster clock drives the logic in the Processor block, where x is 0 to 31.
INTCLKOUT	INTPLLCLK	Coherent Interconnect Clock Clock for the interconnect and other expansion master and slave ports. This clock is generated from INTPLLCLK

Id. at p. 41

4.3 Power control

Good power management is key to reduce system power consumption while maintaining a high performance.

An RD-TC21 reference subsystem contains the following power management features:

- Multiple voltage domains to allow for *Dynamic Voltage and Frequency Scaling* (DVFS) on application processors and the GPU
- Multiple power-gated regions provide comprehensive leakage management
- Multiple power modes for different system scenarios
- A *System Control Processor* (SCP) based on a Cortex®-M3 processor controls power, clock, reset, and the static configuration of the system
- *Power Policy Units* (PPUs) are used to manage power states of each voltage and power domain under the control of the SCP

Id. at 47-48

Claim 1	Accused Products
	4.3.1 Voltage domain A voltage domain is defined as a collection of design elements supplied by a single voltage. The voltage supply to the domain might be scaled or switched off for power or performance reasons. Total Compute 2021 Reference Design (RD-TC21) supports the following voltage domains: **VCPU0** The first voltage domain in the processor cluster for "LITTLE" cores. Supports DVFS. **VCPU1** The second voltage domain in the processor cluster for ELP and "big" cores. Supports DVFS. **VGPU** The voltage domain for GPU. Supports DVFS. **VSYS** The voltage domain for the rest of the subsystem. Does not support DVFS. *Id.* at p. 48 **SCP runtime firmware** The SCP runtime firmware executes after *Trusted Firmware for A-profile* (TF-A) BL2 has authenticated and copied it from flash. The SCP runtime firmware performs the following functions: • Responds to *System Control and Management Interface* (SCMI) messages through *Message Handling Unit* (MHU) version 2.0 for processor power control and *Dynamic Voltage and Frequency Scaling* (DVFS) • Power domain management • Clock management *Id.* at p. 65

Claim 1	Accused Products
	Our initial testing shows that Snapdragon 835's Kryo 280 CPU is an octa-core, big.LITTLE configuration with four semi-custom A73 "performance" cores and four semi-custom A53 "efficiency" cores. Kryo 280's performance cores are pretty much equivalent to Kirin 960's A73 cores in both integer and floating-point IPC, but comparing them to Snapdragon 820's Kryo CPU shows mixed results: integer IPC improves but floating-point regresses. https://www.anandtech.com/show/11201/qualcomm-snapdragon-835-performance-preview/6 **Voltage domains** The voltage supply to a domain might be scaled or removed for power or performance reasons. Except for low complexity solutions, it is rare to use a single logic voltage supply for the whole SoC. The primary reason for additional voltage domains is to support DVFS for functional areas of the SoC. The second reason is to enable external supply switch-off, or reduction to non-functional state retention levels, to some logic areas while maintaining an operational level supply to others. However, the cost for additional voltage domains is significant, because additional voltage regulators, extra effort, and complexity are required in the SoC physical implementation. Therefore, you must carefully assess the value of the addition of each voltage domain against the performance and power requirements for the design. In a big.LITTLE system, each cluster must have a dedicated voltage supply. This is a critical success factor when combined with big.LITTLE software. "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products

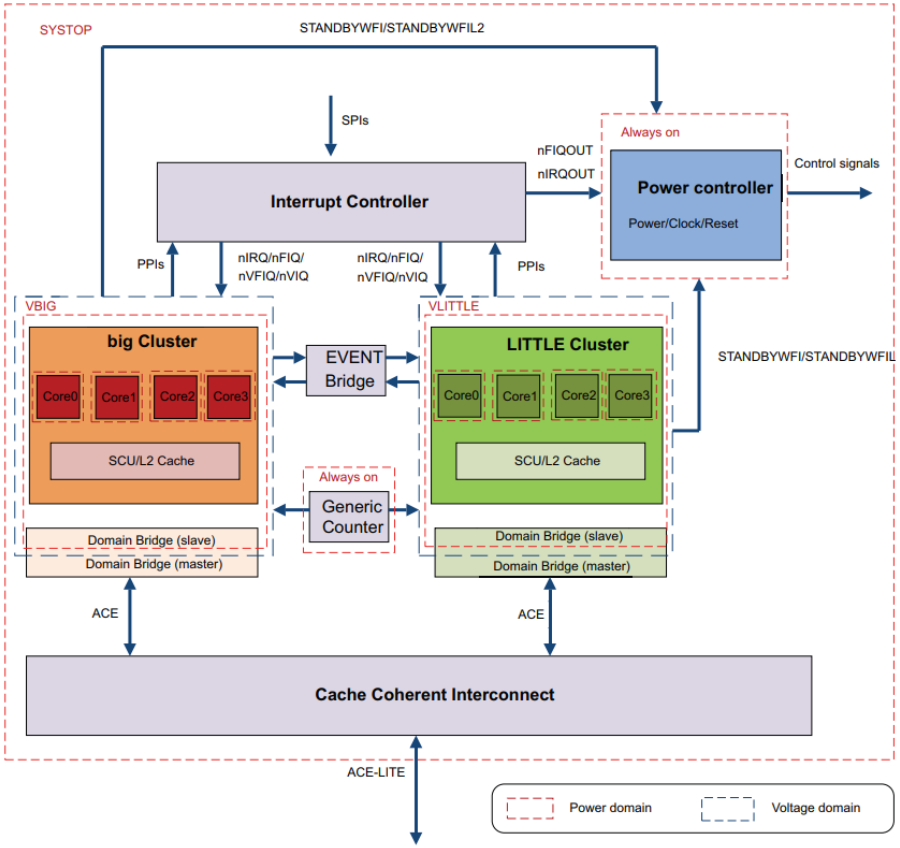
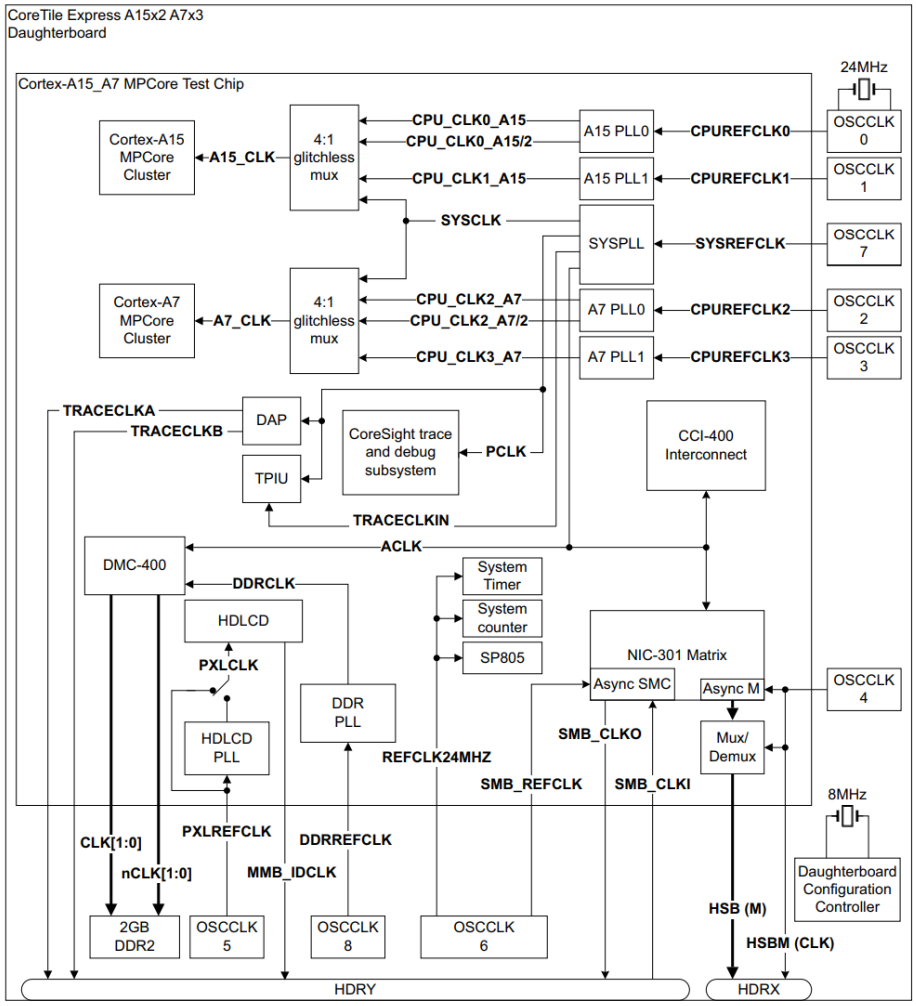


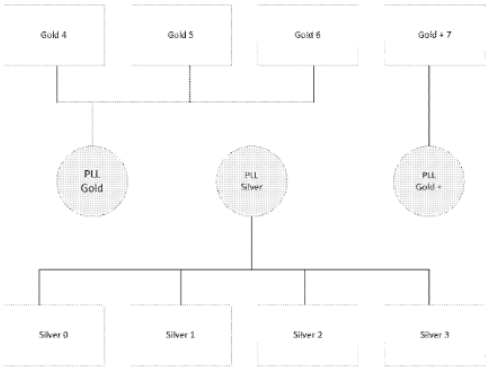
Figure 2-2 Power domain hierarchy

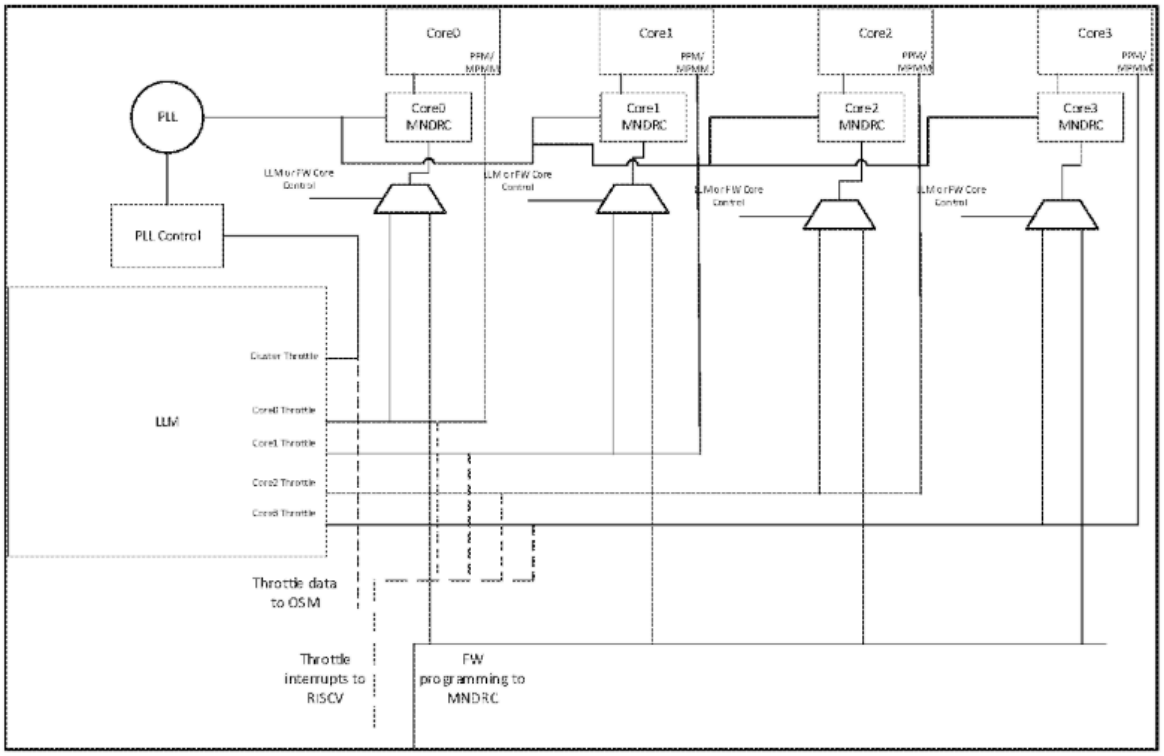
In Figure 2-2, two processor clusters are implemented with per-core and cluster power domains. The big cluster is in the VBIG voltage domain, while the LITTLE cluster is in the VLITTLE voltage domain. The system controller is in an always-on power domain. All the other components are in the system logic power domain (SYSTOP).

"High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products
	Clock domains Clock domains can interact with each other synchronously or asynchronously. Synchronous clock domains can have independent source activity. Each cluster requires an independent clock, and the CCI requires a clock. "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products
	 **Figure 2-10 CoreTile Express A15×2 A7×3 daughterboard clocks** ARM® CoreTile Express A15×2 A7×3 Technical Reference Manual, available at https://developer.arm.com/documentation/ddi0503/i/

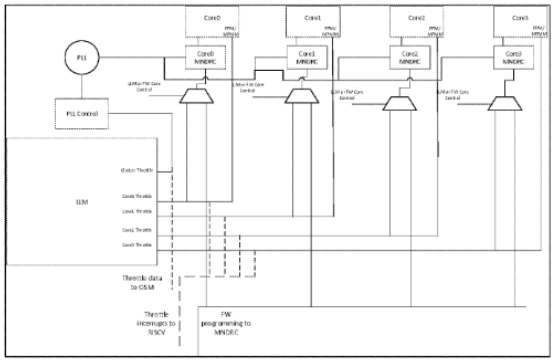
Claim 1	Accused Products
	Qualcomm's documentation demonstrates that the accused devices are configured to contain a first and second set of processor cores according to the above referenced architectures. For example, both the Snapdragon 8 Gen 2 Octa-Core, die code Kailua, and Snapdragon 835 Mobile Platform, MSM8998, are configured with a first set of "Gold" cores and a second set of "Silver" cores, each set having its own PLL Gold or PLL Silver with its own input and output clock signal, and each having a separate power domain and power rails, both the power and output clock signal being variable and the clusters being configured to receive the same: Motivation Current implementation • Current implementation in CPUSS requires that each core per cluster domain run at the same clock frequency. • This requirement is due to the fact that each core doesn't have its own PLL. • OSM aggregates and chooses MAX frequency for operation for those cores. 

Claim 1	Accused Products
	 Kailua

Claim 1	Accused Products

LLM & FW Interaction

- For Kailua implementation the MNDRC's can either be controlled by FW or by LLM directly but not by both.
- When testing for LLM thermal mitigation data the MUX control is switched to LLM that will drive per core MVAL based on it's LUT table.
- When gathering power profile data for SW the MUX control is switched to FW.
- Note that if there is a need to capture data from SW and LLM driven MVAL's to MNDRC then Interrupt driven control is to be used to ensure we have single master that drives MVAL.
- Note that POR implementation for inner and outer loop and per core MPMM/PPM control remains the same.
- The Design has been introduced such that it does not affect POR requirements of LLM and FW



Source sample text

15

Claim 1	Accused Products

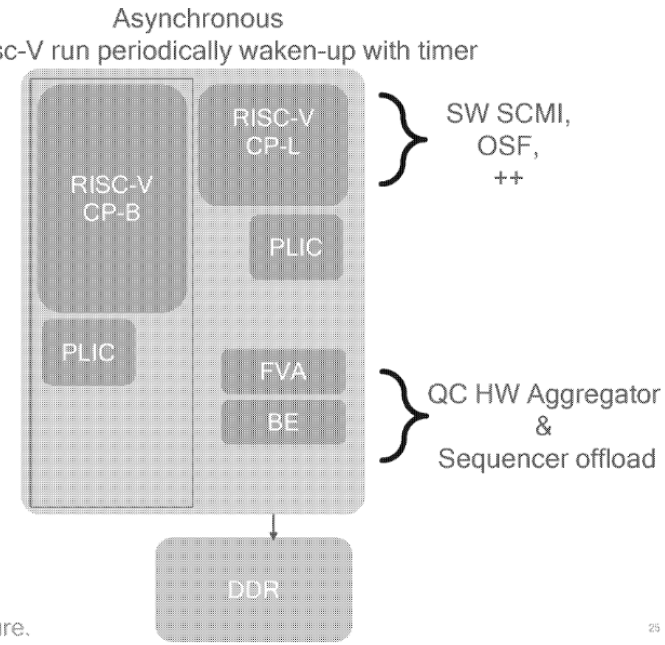
Post Waipio Options: Big and Little RISC-V Split(Azzedine)

Two RISC-Vs :

1. CP-B: High Frequency (Periodic usage - New features to generate data for CP-L of CPU)
2. CP-L: Low Frequency mode
3. Complex features in "Big" RISC-V (CP-B) will not be propagated to VT
4. Big Risc-V is to be designed in a way that is not be product gating
5. Upgrade to SiFive solution is recommended (to leverage opensource SW tools*.)

SW recommendation for premium for experimentation

*Pulp is not fully compliant to the RISC-V architecture.



25

QCREDSTONE_0098870 at -74, -83, -84, -96.

GOLD cluster frequency plan

Mode	PoR Frequency (MHz)	Source (HF PLL)	PLL config							
			VCO freq (MHz)	PLL mode	L Value	PLL div	PLL Power (mW)	Period Jitter (ps)	Half-Cyc jitter (ps)	src_sel
Turbo_L5 CN 0.960V TT/0.960V, SS/xxV	2764	APC1 PLL -early	2764.8	HF	144	1		8.9	23.2	src5
Turbo_L5 0.960V TT/0.960V, SS/xxV	2361	APC1 PLL -early	2361.6	HF	123	1		10.2	26.5	src5
Turbo_L3 CW 0.890V TT/0.890V, SS/0.950V	2361	APC1 PLL -early	2361.6	HF	123	1		10.6	27.5	src5
Turbo_L3 RCW 0.890V TT/0.890V, SS/0.950V	2361	APC1 PLL -early	2361.6	HF	123	1		10.6	27.5	src5

Claim 1	Accused Products

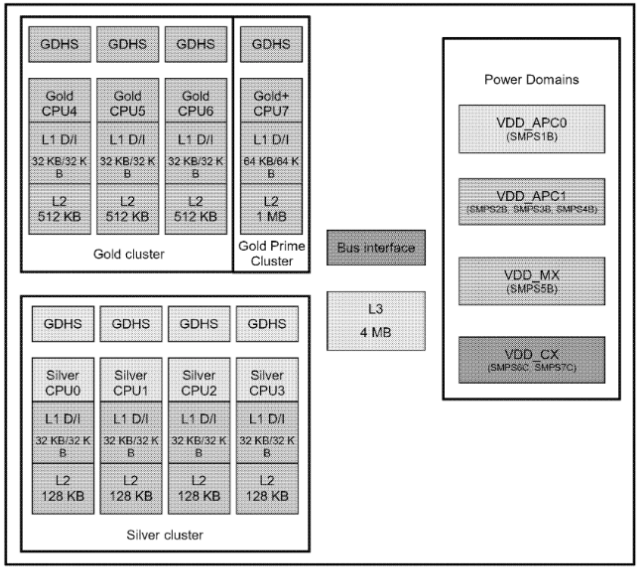
SILVER cluster frequency plan

Mode	PoR Frequency (MHz)	Source (SR PLL)	PLL config							
			VCO freq (MHz)	PLL mode	L Value	PLL div	PLL Power (mW)	Period Jitter (ps)	Half-Cyc jitter (ps)	src_sel
Turbo_L5 CN 0.960V TT/0.960V, SS/xxV	2054	APC0 PLL -early	2054.4	HF	107	1		12.2	31.6	src5
Turbo_L5 0.960V TT/0.960V, SS/xxV	1843	APC0 PLL -early	1843.2	HF	96	1		13.6	35.3	src5
Turbo_L3 CW 0.890V TT/0.890V, SS/0.950V	1843	APC0 PLL -early	1843.2	HF	96	1		13.6	35.3	src5
Turbo_L3 RCW 0.890V TT/0.890V, SS/0.950V	1843	APC0 PLL -early	1843.2	HF	96	1		13.6	35.3	src5
Turbo_L3 CNOM 0.890V TT/0.890V, SS/0.950V	2054	APC0 PLL -early	2054.4	HF	107	1		12.2	31.6	src5
Turbo_L3 0.890V TT/0.890V, SS/0.950V	1843	APC0 PLL -early	1843.2	HF	96	1		13.6	35.3	src5
Turbo_L2 0.800V TT/0.800V, SS/0.860V	1843	APC0 PLL -early	1843.2	HF	96	1		12.2	31.6	src5

QCREDSTONE_0123173 at -73, -77.

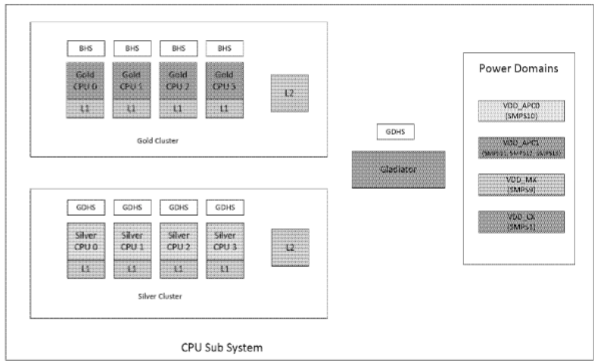
CPUSS

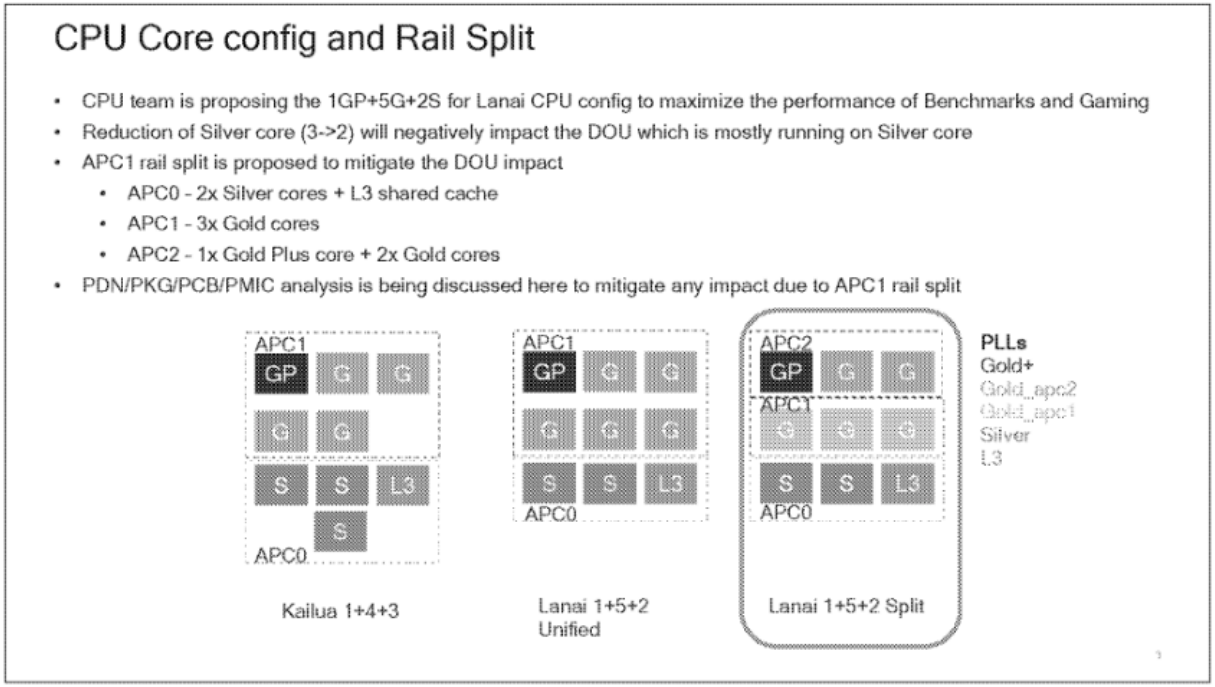
- Kryo 685 Next Gen V8
- Kryo Gold Prime Fmax: 2.6+ GHz
- Kryo Gold Fmax: 2.3+ GHz
- Kryo Silver Fmax: 1.8 GHz
- Kryo Gold Prime L1/L2 cache: 64 KB/1 MB
- Kryo Gold L1/L2 cache: 32 KB/512 KB
- Kryo Silver L1/L2 cache: 32 KB/128 KB
- Frequency of Operation
  - Gold Prime, Gold, Silver, and L3 cache can operate at different frequencies (Independently controlled).
  - Within Silver cluster, all 4 Silver cores and L2 are synchronous.
  - Within Gold cluster, all 3 Gold cores and L2 are synchronous.
  - Within Gold Prime cluster, Gold Prime core and L2 are synchronous
- Power rail
  - Gold Prime core and Gold core share VDD_APC1.
  - Silver core and L3 logic share VDD_APC0.
  - L1 and L2 cache memory cell powered by VDD_MX.
  - Each Kryo Silver/Gold/Gold Prime core has a global distributed head switch (GDHS) to power the core.

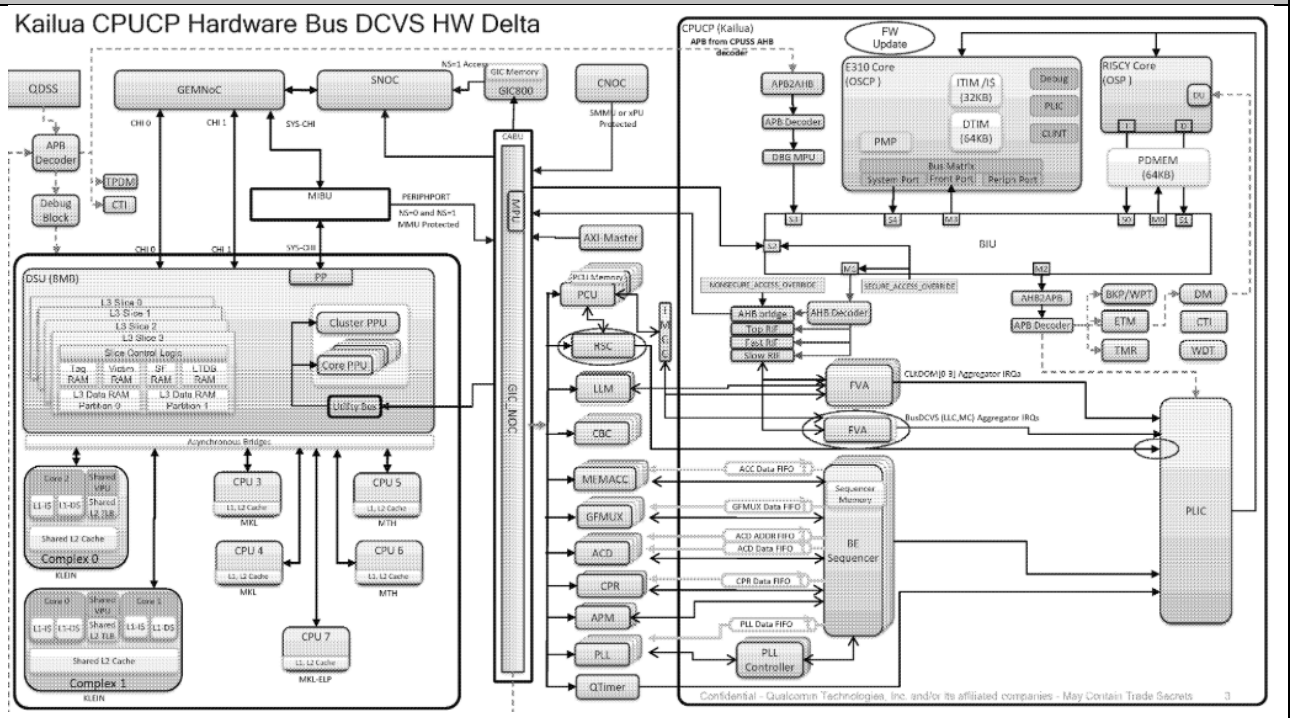


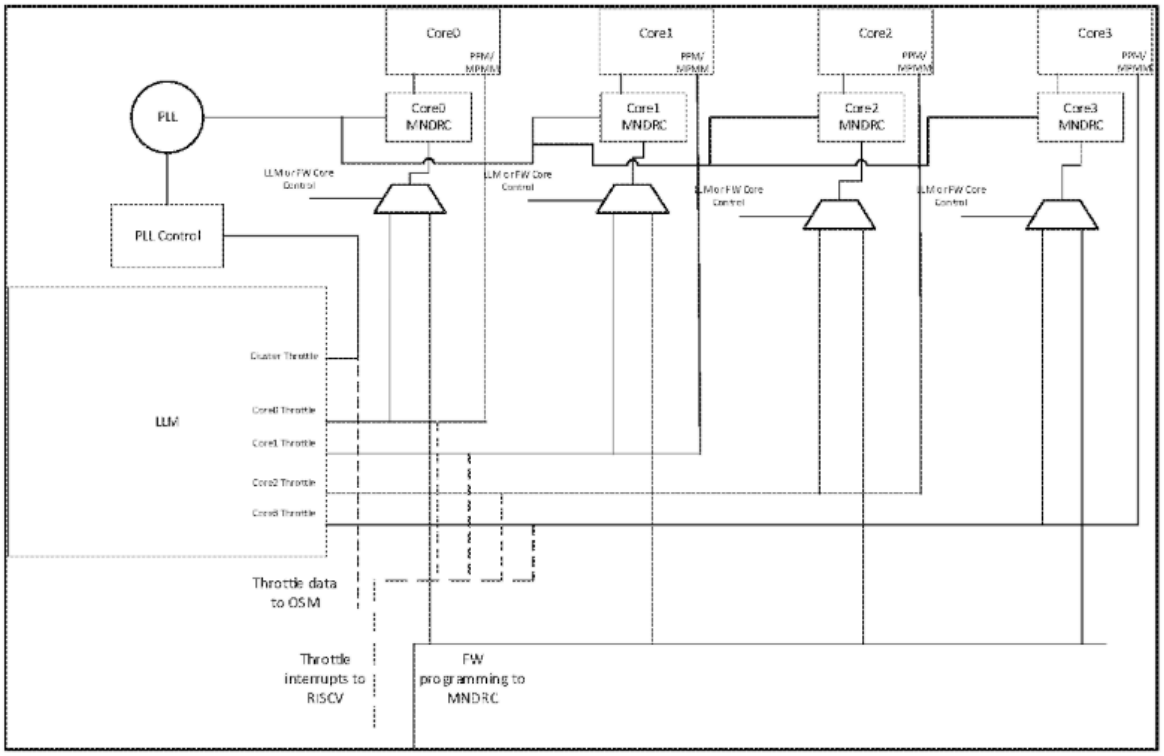
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QCREDSTONE_0039762 at -71

Claim 1	Accused Products
	CPU Power ▪ Customized 64-bit ARM v8-compliant apps processor (Kryo 2xx CPU) ▪ Two Clusters in CPU subsystem – Kryo Gold and Kryo Silver ▪ Kryo Gold Cluster – Quad Kryo high performance CPUs with 2.5 GHz to 2.7 GHz Speed ▪ Kryo Silver Cluster – Quad Kryo low power CPUs with 1.5 GHz to 1.9 GHz Speed ▪ L1 and L2 Cache: ▪ L2 cache at 2 MB for Kryo Gold ▪ L2 cache at 1 MB for Kryo Silver ▪ Power rails: ▪ Kryo Gold cluster and Silver cluster have dedicated, separate power rails ▪ PM8998 SMPS10 powers the Kryo Silver cluster ▪ PM8998 SMPS11/12/13 are tied together as a single trace to power the Kryo Gold cluster ▪ Each Kryo Gold core has a block head switch (BHS) and each Kryo Silver core has a global distributed head switch (GDHS) to power the core ▪ Gold and Silver cluster, along with the respective L2 cache, can operate on a different clock source at different frequencies. ▪ Within a cluster, the cores and L2 are synchronous  QCREDSTONE_0082868 at -878.

Claim 1	Accused Products
	 QCREDSTONE_0091042 at -44.

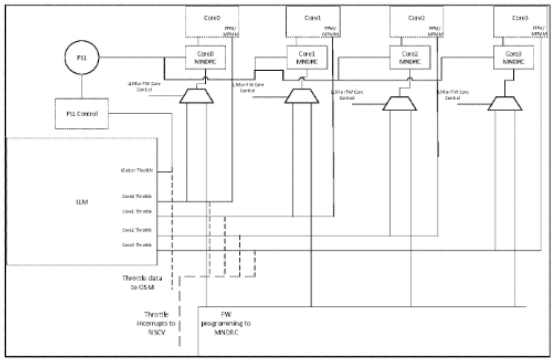
Claim 1	Accused Products
	 QCREDSTONE_0098768 at -70. Additionally, Qualcomm documentation shows that each cluster of cores, e.g. gold and silver, is in a different power domain and clock domain, configured to provide independent voltages and clock signals to each cluster:

Claim 1	Accused Products
	 Kailua

Claim 1	Accused Products

LLM & FW Interaction

- For Kailua implementation the MNDRC's can either be controlled by FW or by LLM directly but not by both.
- When testing for LLM thermal mitigation data the MUX control is switched to LLM that will drive per core MVAL based on it's LUT table.
- When gathering power profile data for SW the MUX control is switched to FW.
- Note that if there is a need to capture data from SW and LLM driven MVAL's to MNDRC then Interrupt driven control is to be used to ensure we have single master that drives MVAL.
- Note that POR implementation for inner and outer loop and per core MPMM/PPM control remains the same.
- The Design has been introduced such that it does not affect POR requirements of LLM and FW



Source sample text

15

Claim 1	Accused Products

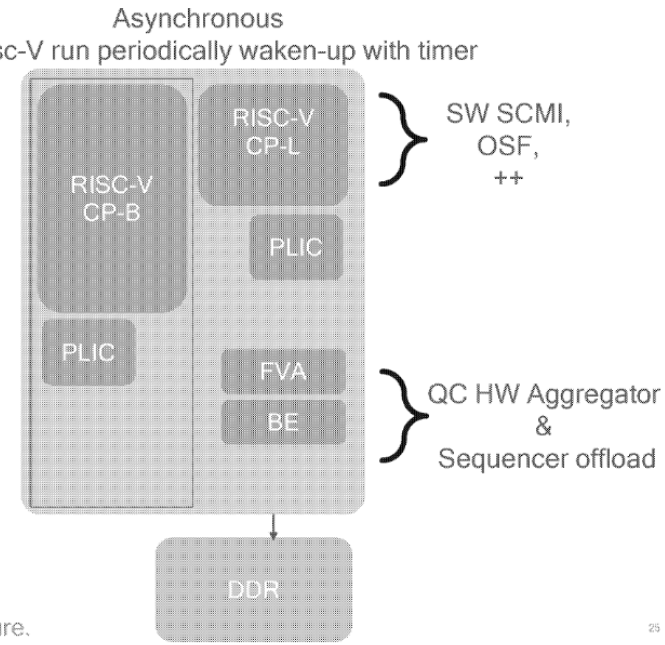
Post Waipio Options: Big and Little RISC-V Split(Azzedine)

Two RISC-Vs :

1. CP-B: High Frequency (Periodic usage - New features to generate data for CP-L of CPU)
2. CP-L: Low Frequency mode
3. Complex features in "Big" RISC-V (CP-B) will not be propagated to VT
4. Big Risc-V is to be designed in a way that is not be product gating
5. Upgrade to SiFive solution is recommended (to leverage opensource SW tools*.)

SW recommendation for premium for experimentation

*Pulp is not fully compliant to the RISC-V architecture.



25

QCREDSTONE_0098870 at -74, -83, -84, -96.

GOLD cluster frequency plan

Mode	PoR Frequency (MHz)	Source (HF PLL)	PLL config							
			VCO freq (MHz)	PLL mode	L Value	PLL div	PLL Power (mW)	Period Jitter (ps)	Half-Cyc jitter (ps)	src_sel
Turbo_L5 CN 0.960V TT/0.960V, SS/xxV	2764	APC1 PLL -early	2764.8	HF	144	1		8.9	23.2	src5
Turbo_L5 0.960V TT/0.960V, SS/xxV	2361	APC1 PLL -early	2361.6	HF	123	1		10.2	26.5	src5
Turbo_L3 CW 0.890V TT/0.890V, SS/0.950V	2361	APC1 PLL -early	2361.6	HF	123	1		10.6	27.5	src5
Turbo_L3 RCW 0.890V TT/0.890V, SS/0.950V	2361	APC1 PLL -early	2361.6	HF	123	1		10.6	27.5	src5

Claim 1	Accused Products

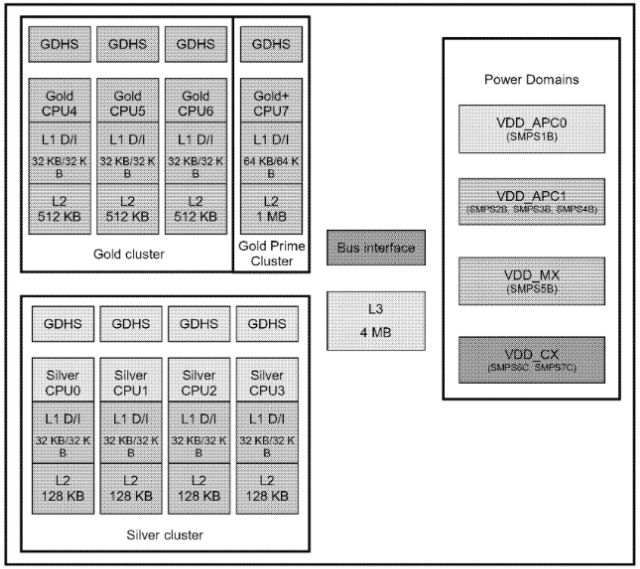
SILVER cluster frequency plan

Mode	PoR Frequency (MHz)	Source (SR PLL)	PLL config							
			VCO freq (MHz)	PLL mode	L Value	PLL div	PLL Power (mW)	Period Jitter (ps)	Half-Cyc jitter (ps)	src_sel
Turbo_L5 CN 0.960V TT/0.960V, SS/xxV	2054	APC0 PLL -early	2054.4	HF	107	1		12.2	31.6	src5
Turbo_L5 0.960V TT/0.960V, SS/xxV	1843	APC0 PLL -early	1843.2	HF	96	1		13.6	35.3	src5
Turbo_L3 CW 0.890V TT/0.890V, SS/0.950V	1843	APC0 PLL -early	1843.2	HF	96	1		13.6	35.3	src5
Turbo_L3 RCW 0.890V TT/0.890V, SS/0.950V	1843	APC0 PLL -early	1843.2	HF	96	1		13.6	35.3	src5
Turbo_L3 CNOM 0.890V TT/0.890V, SS/0.950V	2054	APC0 PLL -early	2054.4	HF	107	1		12.2	31.6	src5
Turbo_L3 0.890V TT/0.890V, SS/0.950V	1843	APC0 PLL -early	1843.2	HF	96	1		13.6	35.3	src5
Turbo_L2 0.800V TT/0.800V, SS/0.860V	1843	APC0 PLL -early	1843.2	HF	96	1		12.2	31.6	src5

QCREDSTONE_0123173 at -73, -77.

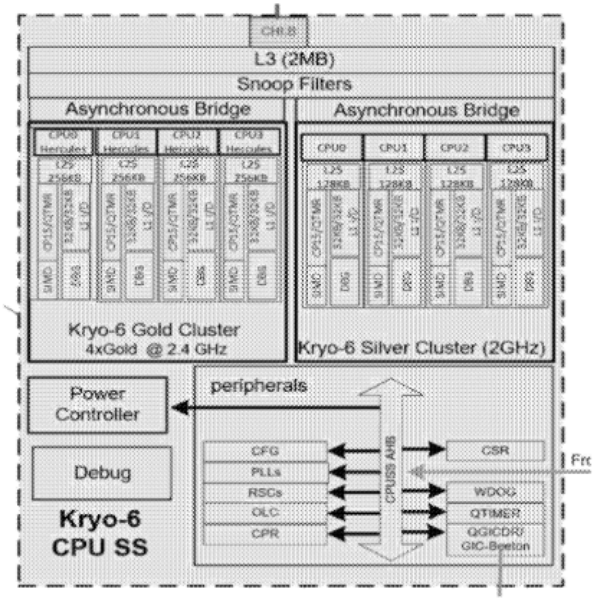
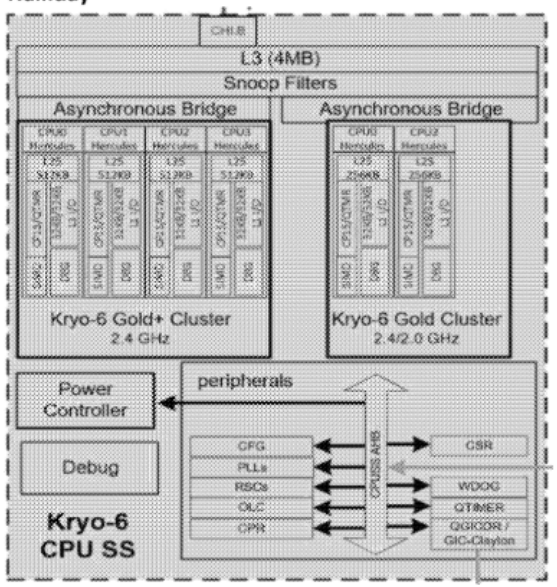
CPUSS

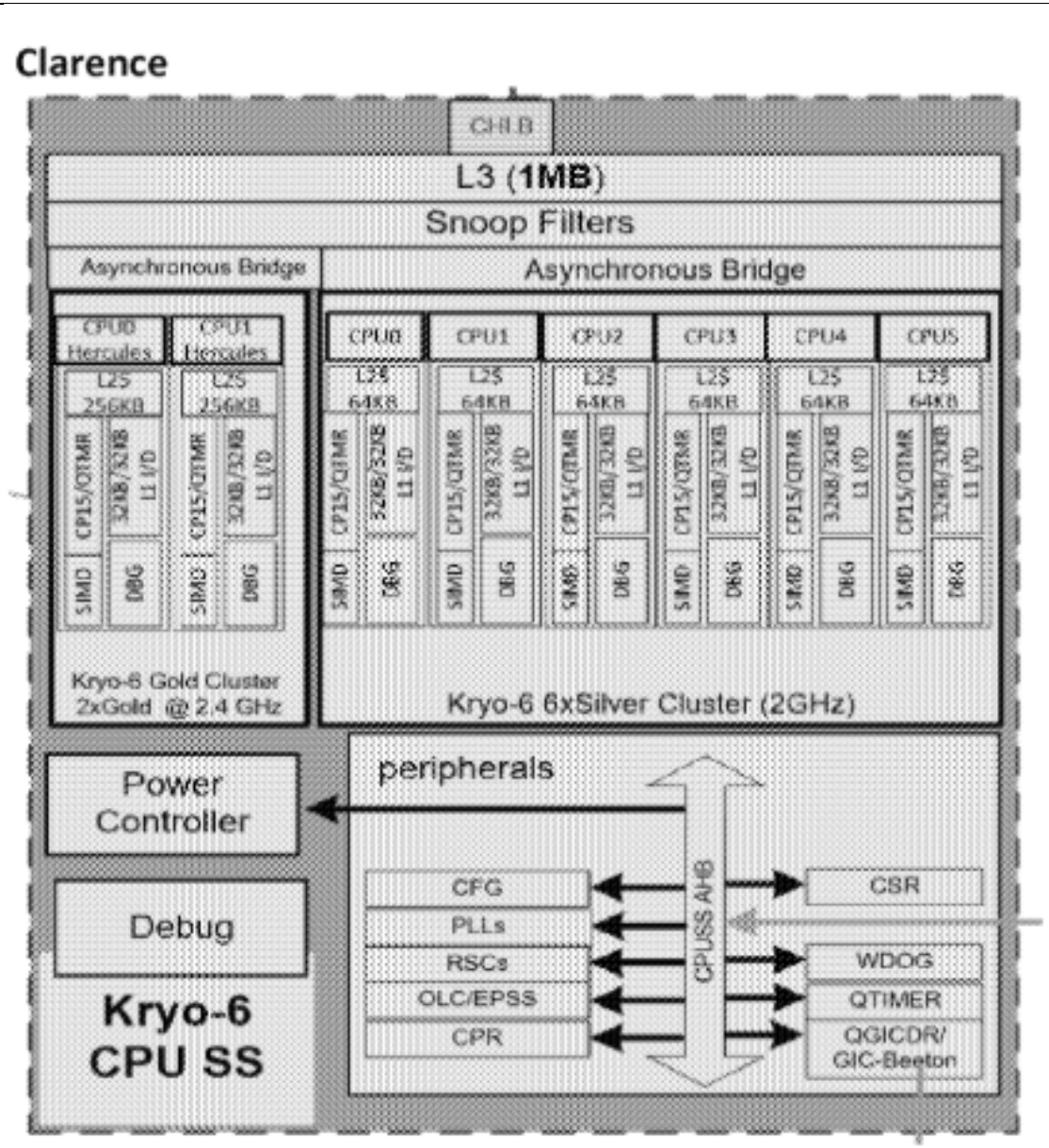
- Kryo 685 Next Gen V8
- Kryo Gold Prime Fmax: 2.6+ GHz
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- Kryo Silver Fmax: 1.8 GHz
- Kryo Gold Prime L1/L2 cache: 64 KB/1 MB
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  - Within Gold cluster, all 3 Gold cores and L2 are synchronous.
  - Within Gold Prime cluster, Gold Prime core and L2 are synchronous
- Power rail
  - Gold Prime core and Gold core share VDD_APC1.
  - Silver core and L3 logic share VDD_APC0.
  - L1 and L2 cache memory cell powered by VDD_MX.
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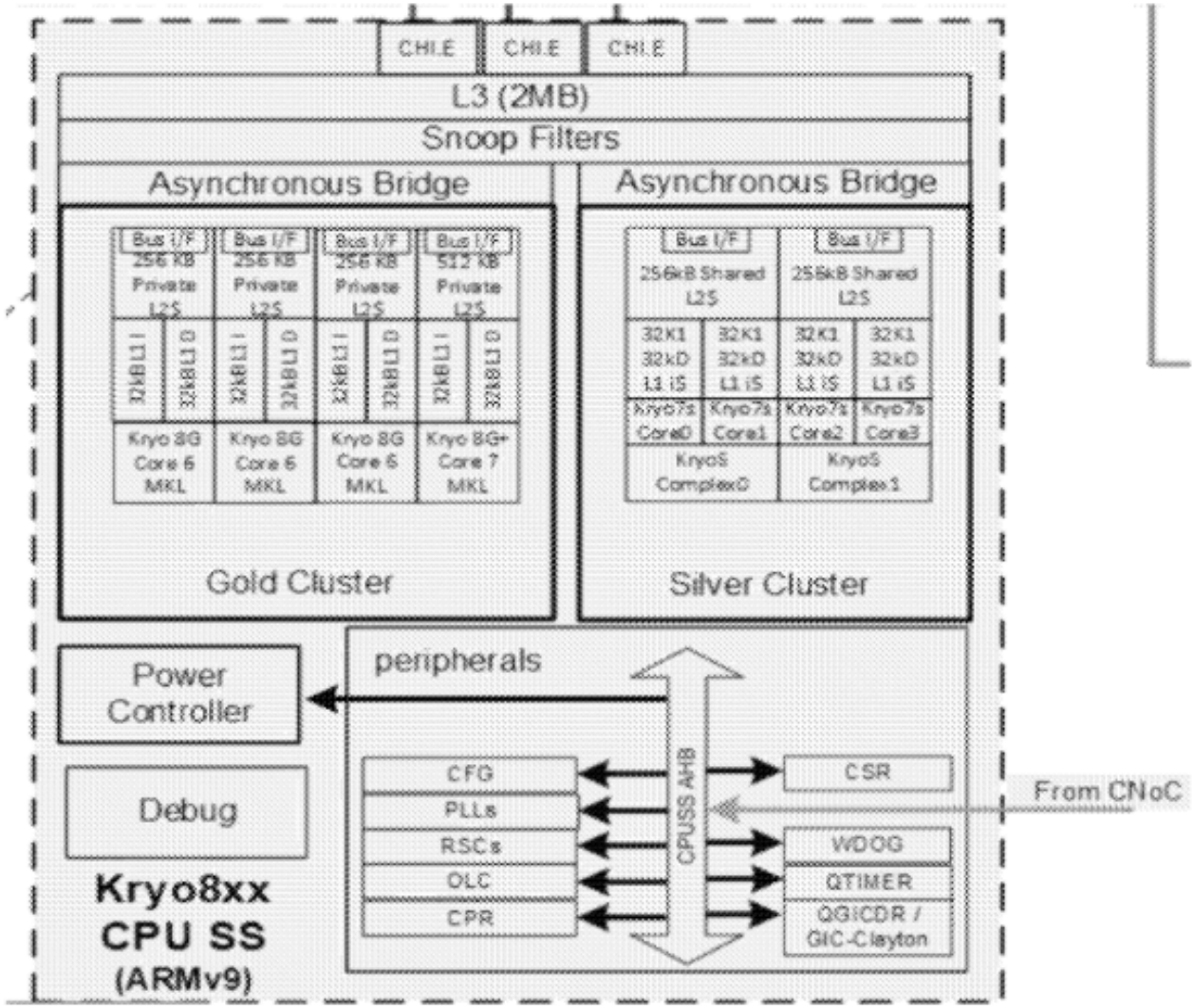


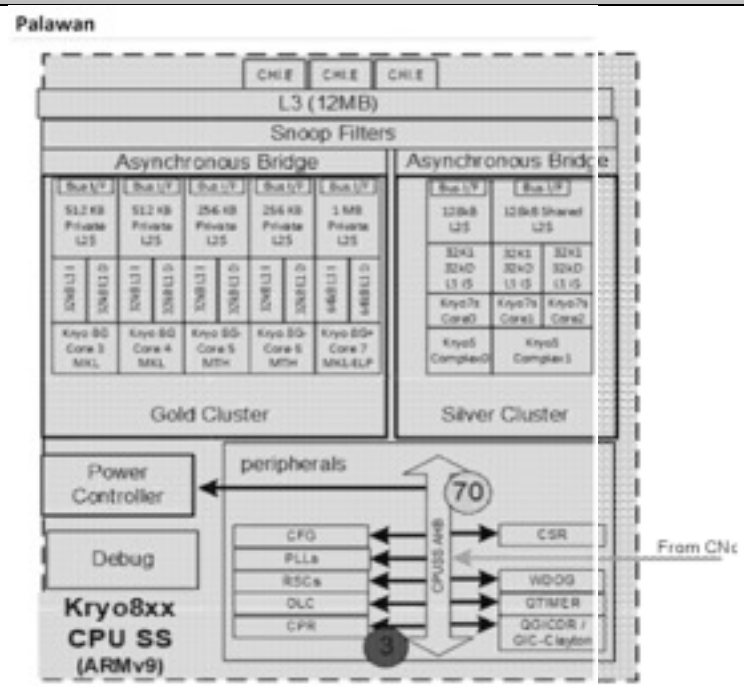
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QCREDSTONE_0039762 at -71

Claim 1	Accused Products
	This arrangement of Gold+, Gold, and/or Silver cores arranged into clusters according to the above referenced architectures is repeated throughout the accused products: Netrani  Halliday 


Clarence
CHUB
L3 (1MB)
Snoop Filters
Asynchronous Bridge
Asynchronous Bridge
CPU0 Hercules
CPU1 Hercules
L2$ 256KB
CP15/QTIMR
32KB/32KB L1 I/D
SIMD
DBG
CPU0
CPU1
CPU2
CPU3
CPU4
CPU5
L2$ 64KB
Kryo-6 Gold Cluster 2xGold @ 2.4 GHz
Kryo-6 6xSilver Cluster (2GHz)
Power Controller
peripherals
Debug
Kryo-6 CPU SS
CFG
PLLs
RSCs
OLC/EPSS
CPR
CPUSS AHB
CSR
WDOG
QTIMER
QGICDR/ GIC-Beeton

Claim 1	Accused Products
	

Claim 1	Accused Products
	 QCREDSTONE_0098556 at -558 to -562.

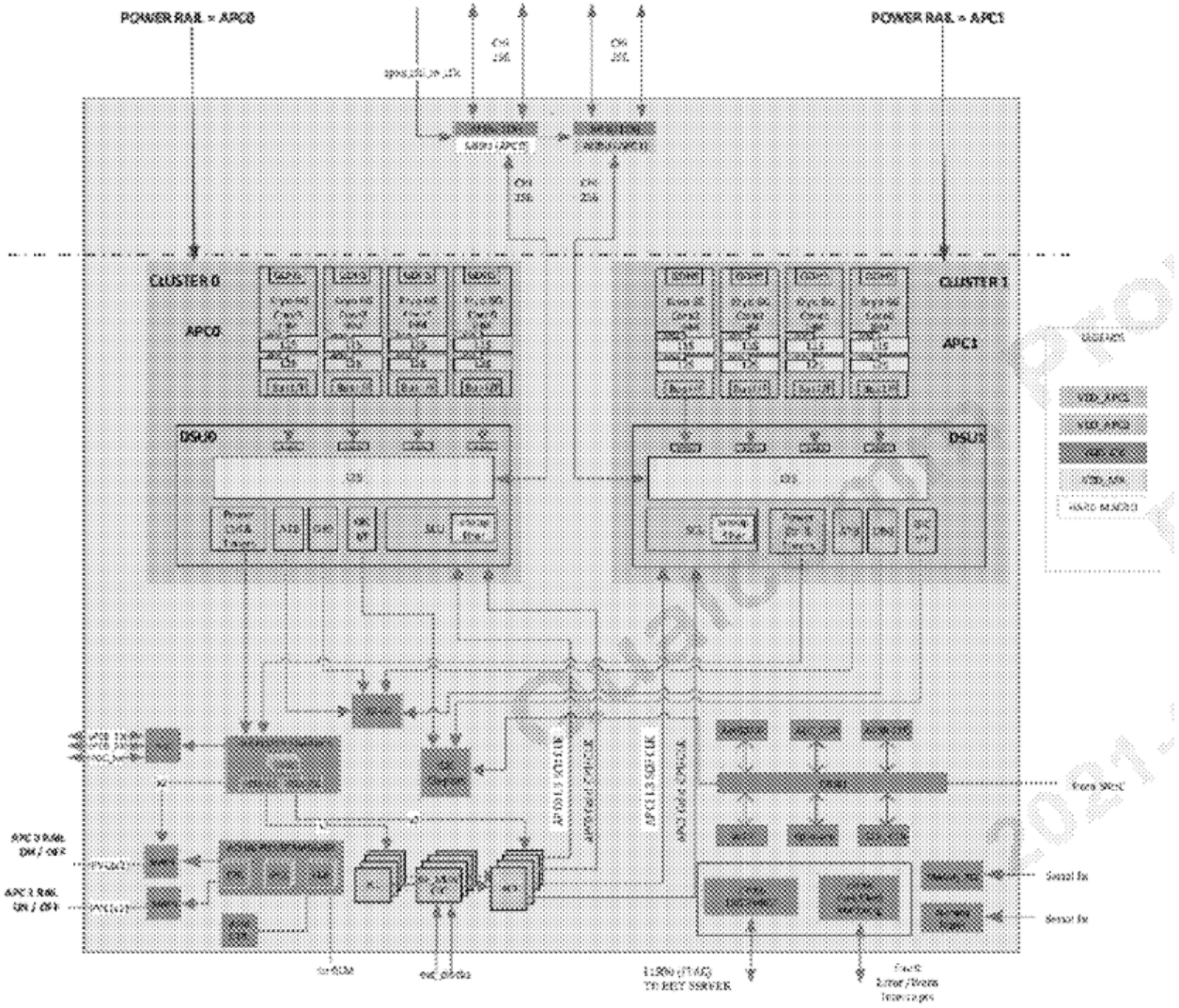
Claim 1	Accused Products

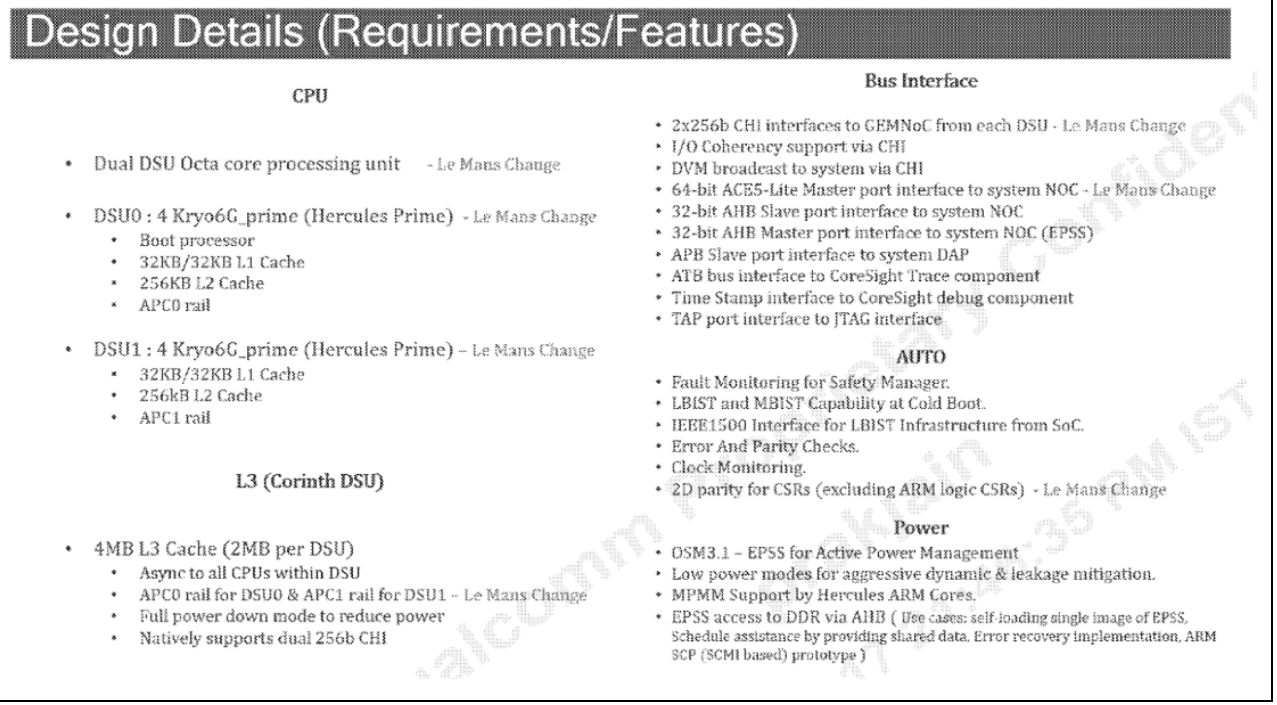
DSU Configuration

Kryo6 L3

Parameter name	Permitted values	Selection	Description
NUM_BIG_CORES	0 to 8	4	3 Gold + 1 Gold+
NUM_LITTLE_CORES	0 to 8	4	4 Silver Cores
CHI	TRUE/FALSE	TRUE	Corinth cluster to the Gladiator interconnect interface is CHI
MASTER DATA_WIDTH	128/256	256	2x128bit wide CHI port to the Gladiator interconnect
L3_CACHE	TRUE/FALSE	TRUE	Include L3 Cache
ACP	TRUE/FALSE	FALSE	ACP interface not included on the Corinth cluster
PERIPH_PORT	TRUE/FASLE	TRUE	Peripheral port not included on the Corinth Cluster
SCU_CACHE_PROTECTION	TRUE/FALSE	TRUE	Protect the L3 Cache RAMs and snoop filter RAMs with ECC
L3_CACHE_SIZE	512/1024/2048/4096KB	4096KB	4M L3 cache
L3_DATA_WR_LATENCY	1 or 2	2	L3 Data RAM input latency is 1 cycle
L3_DATA_RD_LATENCY	2 or 3	2	L3 Data RAM output latency is 2 cycle

QCREDSTONE_0090058 at -71.

Claim 1	Accused Products
	

Claim 1	Accused Products
	

Claim 1	Accused Products

3rd Party

Third Party IPs (3PIP) and Export Controlled IP

Do you have any 3rd Party IPs to declare? (note that this is a sign-off on the accuracy of your answer, which may have financial implications):
YES

Supplier	Licensed IP Description	# Instances	Changed from Previous Program (Y/N)?	QCOM Owner	Delta Comments
Arm Limited	Hercules Processor/Hercules Crypto/HerculesPrime Processor/HerculesPrime Crypto/Dynamiq Shared Unit 8MB Version (DSU 8MB)	8	yes		L1/L2 size changed from 64KB/512KB to 32KB/256KB
Arm Limited	Hercules Processor/Hercules Crypto/HerculesPrime Processor/HerculesPrime Crypto/Dynamiq Shared Unit 8MB Version (DSU 8MB)	2	yes		L3 size changed from 8MB to 2MB (per cluster)
Arm Limited	GIC-Clayton Generic Interrupt Controller	1	yes		GIC Beeton is replaced with GIC Clayton
Arm Limited	Coresight Components-Various	1	no		
PULP Platform	RI5CY RISC-V Core (Open Source Hardware Platform) https://www.pulp-platform.org/	1	no		

QCREDSTONE_0091177 at -86-87, -248.

GOLD_PLUS frequency plan										
Mode	PoR Frequency (MHz)	Source (HF PLL)	PLL config							
			VCO freq (MHz)	PLL mode	L Value	PLL div	PLL Power (mW)	Period Jitter (ps)	Half-Cyc jitter (ps)	src_sel
Turbo_L5 CN 0.960V TT/0.960V, SS/xxV	2956	APC1 PLL -early	2956.8	HF	154	1		8.5	22.0	src5
Turbo_L5 0.960V TT/0.960V, SS/xxV	2572	APC1 PLL -early	2572.8	HF	134	1		10.0	26.0	src5
Turbo_L3 CW 0.890V TT/0.890V, SS/0.950V	2457	APC1 PLL -early	2457.6	HF	128	1		10.3	26.7	src5

GOLD cluster frequency plan										
Mode	PoR Frequency (MHz)	Source (HF PLL)	PLL config							
			VCO freq (MHz)	PLL mode	L Value	PLL div	PLL Power (mW)	Period Jitter (ps)	Half-Cyc jitter (ps)	src_sel
Turbo_L5 CN 0.960V TT/0.960V, SS/xxV	2764	APC1 PLL -early	2764.8	HF	144	1		8.9	23.2	src5
Turbo_L5 0.960V TT/0.960V, SS/xxV	2361	APC1 PLL -early	2361.6	HF	123	1		10.2	26.5	src5

Claim 1	Accused Products

SILVER cluster frequency plan

Mode	PoR Frequency (MHz)	Source (SR PLL)	PLL config							
			VCO freq (MHz)	PLL mode	L Value	PLL div	PLL Power (mW)	Period Jitter (ps)	Half-Cyc jitter (ps)	src_sel
Turbo_L5 CN 0.960V TT/0.960V, SS/xxV	2054	APCO PLL -early	2054.4	HF	107	1		12.2	31.6	src5
Turbo_L5 0.960V TT/0.960V, SS/xxV	1843	APCO PLL -early	1843.2	HF	96	1		13.6	35.3	src5
Turbo_L3 CW 0.890V TT/0.890V, SS/0.950V	1843	APCO PLL -early	1843.2	HF	96	1		13.6	35.3	src5

PLL						
	APSS_CC_SILVER_PLL	apss_cc_silver_pll	1344.00	PLL_SILVER_NOM	1	1478.40
	APSS_CC_SILVER_PLL_EARLY_GRP	apss_cc_silver_pll_out_main	1344.00	PLL_SILVER_NOM	1	1478.40
	APSS_CC_SILVER_PLL_MAIN_GRP	apss_cc_silver_pll_out_even	1344.00	PLL_SILVER_NOM	1	1478.40
	APSS_CC_SILVER_PLL_TEST_GRP	apss_cc_silver_pll_out_test	1344.00	PLL_SILVER_NOM	1	1478.40
	APSS_CC_GOLD_PLL	apss_cc_gold_pll	1401.60	PLL_GOLD_NOM	1	1593.60
	APSS_CC_GOLD_PLL_EARLY_GRP	apss_cc_gold_pll_out_main	1401.60	PLL_GOLD_NOM	1	1593.60
	APSS_CC_GOLD_PLL_MAIN_GRP	apss_cc_gold_pll_out_even	1401.60	PLL_GOLD_NOM	1	1593.60
	APSS_CC_GOLD_PLL_TEST_GRP	apss_cc_gold_pll_out_test	1401.60	PLL_GOLD_NOM	1	1593.60
	APSS_CC_L3_PLL	apss_cc_l3_pll	1209.60	PLL_L3_NOM	1	1344.00
	APSS_CC_L3_PLL_EARLY_GRP	apss_cc_l3_pll_out_main	1209.60	PLL_L3_NOM	1	1344.00
	APSS_CC_L3_PLL_MAIN_GRP	apss_cc_l3_pll_out_even	1209.60	PLL_L3_NOM	1	1344.00
	APSS_CC_L3_PLL_TEST_GRP	apss_cc_l3_pll_out_test	1209.60	PLL_L3_NOM	1	1344.00
	APSS_CC_GOLD_PLUS_PLL	apss_cc_gold_plus_pll	1459.20	PLL_GOLD_PLUS_NOM	1	1651.20
	APSS_CC_GOLD_PLUS_PLL_EARLY_GRP	apss_cc_gold_plus_pll_out_main	1459.20	PLL_GOLD_PLUS_NOM	1	1651.20
	APSS_CC_GOLD_PLUS_PLL_MAIN_GRP	apss_cc_gold_plus_pll_out_even	1459.20	PLL_GOLD_PLUS_NOM	1	1651.20
	APSS_CC_GOLD_PLUS_PLL_TEST_GRP	apss_cc_gold_plus_pll_out_test	1459.20	PLL_GOLD_PLUS_NOM	1	1651.20

Claim 1	Accused Products

Clock Source Data	PLL Fractional or Integer Multiplication					
Root Clock Src	PLL L	PLL M	PLL N	Frequency (MHz)	Source Period Jitter (ns)	Duty Cycle Jitter (ns)
Tester				40.00	0.500	0.500
XO				19.20	0.500	0.500
SLEEP_CLK				0.03	0.500	0.500
PLL_GOLD_CW	123	0	1	2361.60	0.0106	0.0275
PLL_GOLD_RCW	123	0	1	2361.60	0.0106	0.0275
PLL_GOLD_CNOM	141	0	1	2707.20	0.0092	0.0240
PLL_GOLD_TURBO_L1	108	0	1	2073.60	0.0121	0.0314
PLL_GOLD_TURBO_L0	95	0	1	1824.00	0.0137	0.0356
PLL_GOLD_NOM_L1	83	0	1	1593.60	0.0155	0.0403
PLL_GOLD_NOM	73	0	1	1401.60	0.0178	0.0464
PLL_GOLD_SVS_L1	62	0	1	1190.40	0.0210	0.0630
PLL_GOLD_SVS	49	0	1	940.80	0.0372	0.0798
PLL_GOLD_SVS2	33	0	1	633.60	0.0711	0.1343
PLL_GOLD_SVS3	6	0	1	115.20	0.0883	0.1488
PLL_SILVER_CW	96	0	1	1843.20	0.0136	0.0353
PLL_SILVER_RCW	96	0	1	1843.20	0.0136	0.0353
PLL_SILVER_CNOM	107	0	1	2054.40	0.0122	0.0316
PLL_SILVER_TURBO_L1	96	0	1	1843.20	0.0136	0.0353
PLL_SILVER_TURBO_L0	89	0	1	1708.80	0.0146	0.0381
PLL_SILVER_NOM_L1	77	0	1	1478.40	0.0167	0.0434
PLL_SILVER_NOM	70	0	1	1344.00	0.0186	0.0484
PLL_SILVER_SVS_L1	58	0	1	1113.60	0.0227	0.0587
PLL_SILVER_SVS	47	0	1	902.40	0.0388	0.0831
PLL_SILVER_SVS2	31	0	1	595.20	0.0341	0.0341
PLL_SILVER_SVS3	6	0	1	115.20	0.0883	0.1488
PLL_L3_CW	83	0	1	1593.60	0.0157	0.0408
PLL_L3_RCW	83	0	1	1593.60	0.0157	0.0408
PLL_L3_CNOM	94	0	1	1804.80	0.0139	0.0360
PLL_L3_TURBO_L1	83	0	1	1593.60	0.0157	0.0408
PLL_L3_TURBO_L0	78	0	1	1497.60	0.0167	0.0434
PLL_L3_NOM_L1	70	0	1	1344.00	0.0186	0.0484
PLL_L3_NOM	63	0	1	1209.60	0.0207	0.0538
PLL_L3_SVS_L1	52	0	1	998.40	0.0351	0.0744
PLL_L3_SVS	42	0	1	806.40	0.0437	0.0933
PLL_L3_SVS2	27	0	1	518.40	0.0549	0.0549
PLL_L3_SVS3	6	0	1	115.20	0.0883	0.1488
PLL_GOLD_TEST	54	0	1	2073.60	0.0121	0.0314
PLL_SILVER_TEST	54	0	1	1843.20	0.0136	0.0353

QCREDSTONE_0123173 at -173 to -177, -183, -316. *See also* QCREDSTONE_0108055, QCREDSTONE_010943, QCREDSTONE_0110523, QCREDSTONE_0112461, QCREDSTONE_0113841, QCREDSTONE_0114427, QCREDSTONE_0115813, QCREDSTONE_0116536, QCREDSTONE_0117594; QCREDSTONE_0120263, QCREDSTONE_0124233, QCREDSTONE_0125186, QCREDSTONE_0131099.

Claim 1	Accused Products
	Power Model PEU • Dynamic power model: • Pdyn = α * IPC * V^2 * f • Alpha value is tuned per corner (LowSVS, SVS, …, Nominal, …, Turbo) • GoldPlus and Gold: 9 alpha values each • Silver: 6 alpha values **Power Model** PEU • Registers: • **Voltage:** APSS_SILVER_CPRh_STATUS_[0-1] / APSS_GOLD_CPRh_STATUS_[0-1] • DCVSh_corner_last_voltage • **Frequency:** EPSSSLOW_CLKDOM[0/1/2/3]_DOMAIN_STATE • LVAL • **Temperature:** APSS_SILVER_LMH_LLM_TEMP_RX_STS_0_i / APSS_GOLD_LMH_LLM_TEMP_RX_STS_0_i • **IPC:** PMU registers - Instructions and cycles (PMEVCNTR0_EL0, PMCCNTR_EL0) QCREDSTONE_0099078 at -82 to -83.

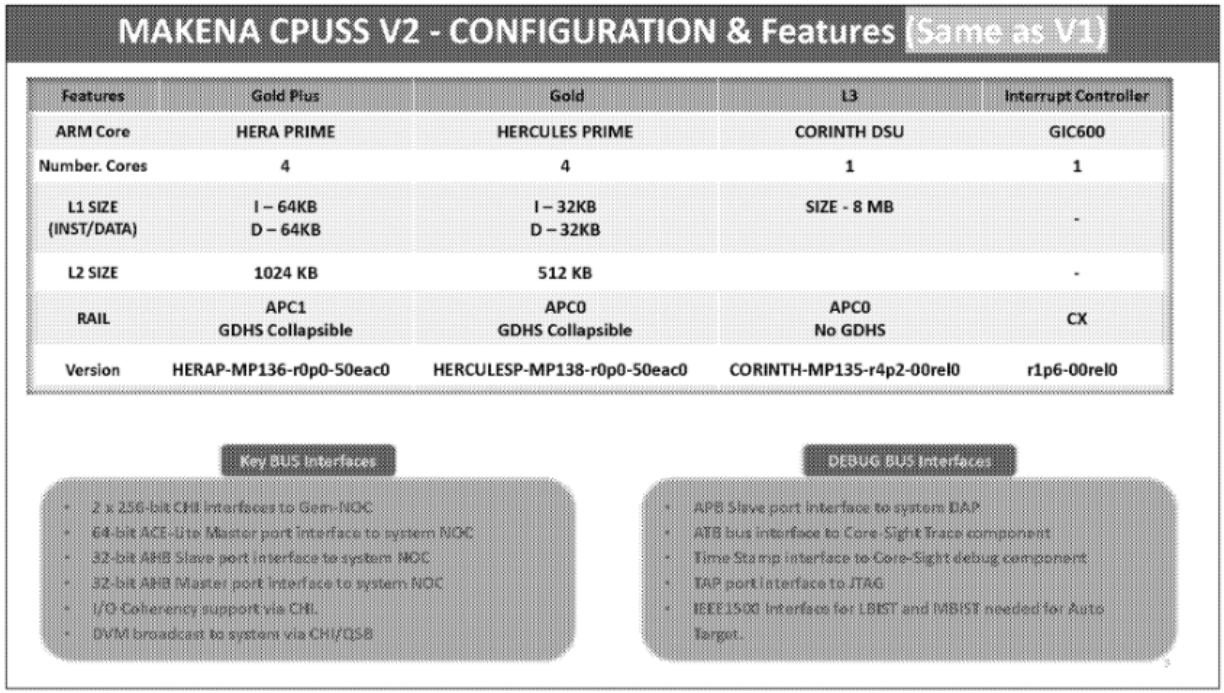
Claim 1	Accused Products

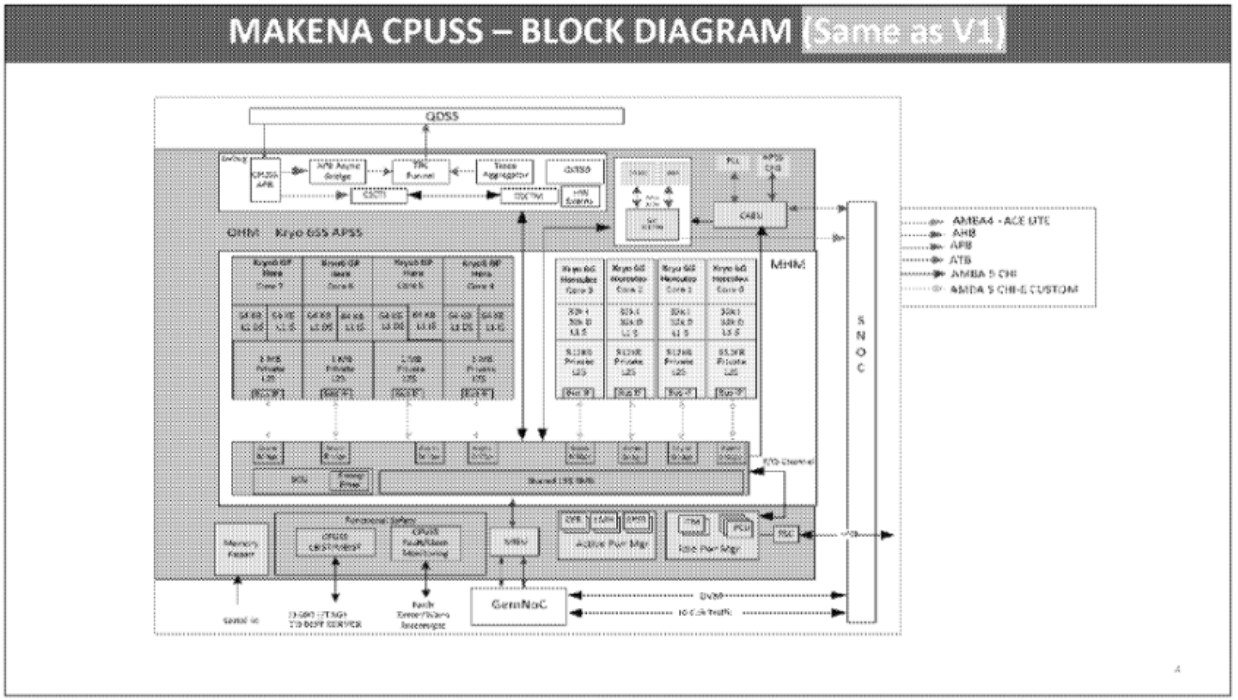
Lanai R2 pre-silicon performance validation

Configuration

Chipset	Kailua R2 RUMI Pre-silicon [illegible]	Lanai V1 RUMI Pre-silicon [illegible]	Lanai R2 RUMI Pre-silicon [illegible]
GOLD+ Frequency (MHz)	1xMKL-ELP@2838.9	1xHUNTER-ELP@2885.1	1xHUNTER-ELP@2885.1
GOLD Frequency (MHz)	2xMKL/2xMTH@2620.7	5xHUNTER@2589.2	5xHUNTER@2589.2
SILVER Frequency (MHz)	3xKlein@2197.9	2xHayes@2148.5	2xHayes@2148.5
L3 Frequency (MHz)	1892.7	1905.3	1905.3
LLC Frequency (MHz)	1064.6	1062.9	1062.9
DDR Frequency (MHz)	4260.2	4207.8	4207.8
Gold +: Cache Size [L2/L1i/L1d] KB	1024/64/64	2048/64/64	2048/64/64
Gold (MTH): Cache Size [L2/L1i/L1d] KB	256/32/32	-	-
Gold (MKL/HUNTER): Cache Size [L2/L1i/L1d] KB	512/32/32	512/64/64	512/64/64
Silver(complex): Cache Size [L2/L1i/L1d] KB	128*/32/32	512*/64/64	512*/64/64
Silver(single): Cache Size [L2/L1i/L1d] KB	128/32/32	-	-
L3: Cache Size MB	8	12	12
LLC: Cache Size MB	6(3 for CPU)	8(5 for CPU)	(5 for CPU)
DDRSS	4ch LP5	4ch LP5	4ch LP5
Build	E3.0	E3.5 (RUMI.V1.SOC.EPSILON4_LPDDR5_GPU)	RUMI.R2.SOC.ALPHA1_LPDDR5
Convex version	convex_2021_08_20_ver_03_09	convex_2022_06_16_ver_03.14	r2_convex_sandbox(early stage)

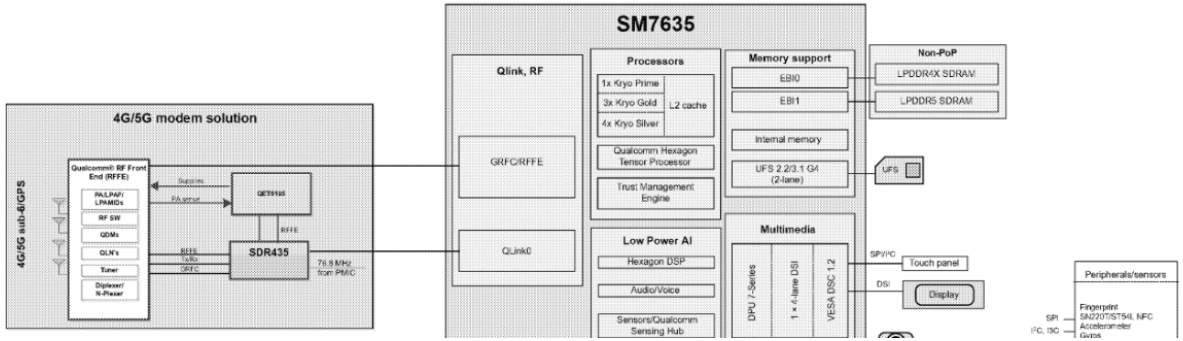
QCREDSTONE_0090953 at -84.

Claim 1	Accused Products
	

Claim 1	Accused Products
	 QCREDSTONE_0092294 at -96, -97.

Claim 1	Accused Products

1.1 Functional block diagram



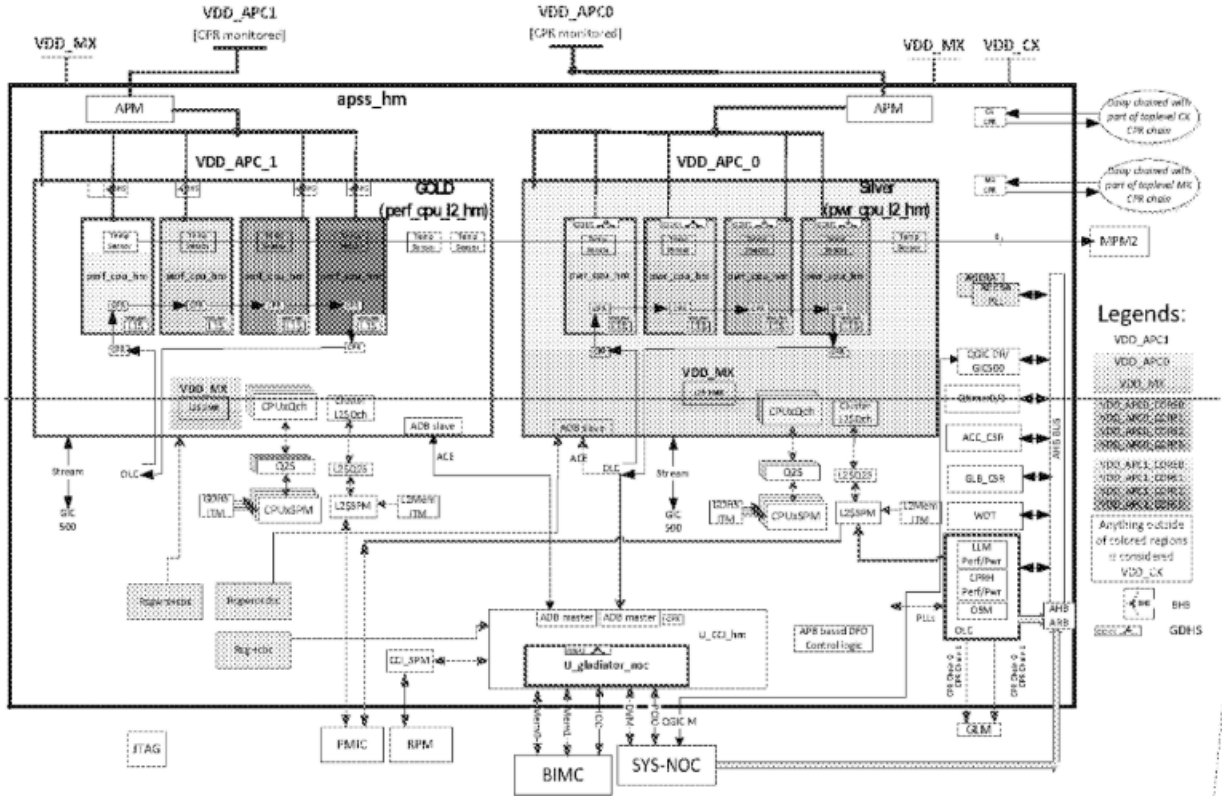
1.2 SM7635 features

NOTE Some of the hardware features integrated within the SM7635 must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SM7635 features.

Table 1-1 SM7635 features

Feature	SM7635 capability
Processors	
Applications	▪ Kryo CPU 7-Series built on Arm Cortex technology ▫ Kryo Prime: One high-performance core ▫ Kryo Gold: Three high-performance cores ▫ Kryo Silver: Four low-power cores

QCREDSTONE_0013455 At -64, -65.

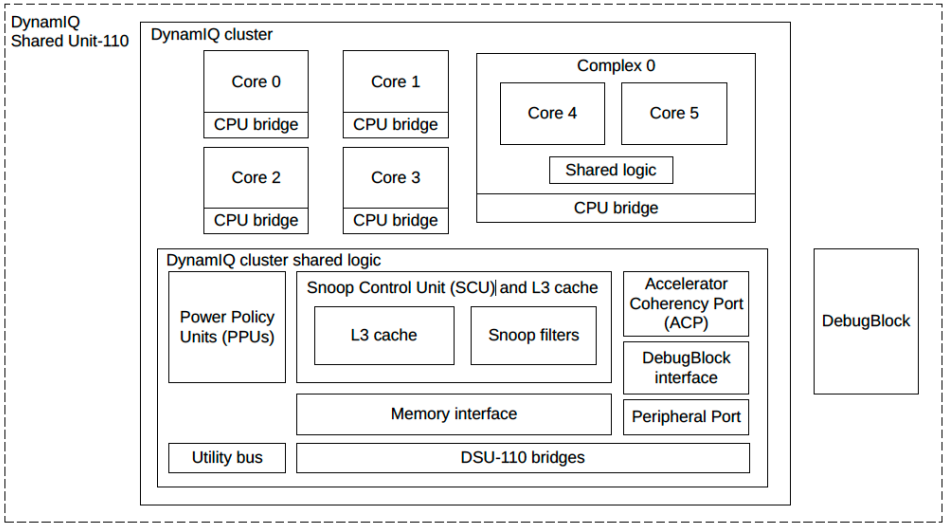
Claim 1	Accused Products
	 QCREDSTONE_0096091 at -104.
[1c] an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the	Each Accused Product comprises an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores. For example, the Snapdragon 8 Gen 2 Octa-Core includes a DynamIQ Shared Unit (DSU), including a Snoop Control Unit (SCU), that is coupled to each core or to each set of processor cores and is configured to communicate between the sets of processor cores, including by

Claim 1	Accused Products
first set of processor cores and the second set of processor cores.	buffering and resynchronizing signals across clock domains and by maintaining coherency between caches in the cores or complexes and/or with the L3 shared memory implemented by the DSU. For another example, the Snapdragon 835 Mobile Platform includes a cache coherent interconnect, such as a CCI-400 or CCI-550, that is coupled to each core or to each set of processor cores and is configured to communicate between the sets of processor cores, for example by maintaining coherency between caches in the cores or complexes. As shown in the relevant documentation, described above and reiterated here for the avoidance of all possible doubt, the Accused Products implement either the big.LITTLE or DynamIQ architecture, which are the heterogeneous processing architectures for the ARM Cortex-A53/A72 and ARM Cortex-A510/A710/A715 respectively. The big.LITTLE architecture is also the heterogenous processing architecture for the ARM Cortex-A7 and Cortex-A15 processors. For example, ARM documentation for the big.LITTLE architecture expressly includes all four of these processors in its stated scope. ARM's public documentation of the big.LITTLE architecture describes the infringing cache coherent interconnect in general, and also in the context of a "typical big.LITTLE system" featuring Cortex-A7 and Cortex-A15 processors. There is a reasonable inference that ARM's document also applies to the Accused Products with big.LITTLE architectures including Cortex-A53 and Cortex-A72 cores. And the ARM documentation for the ARM Cortex-A510 processor core expressly states that it includes and supports the DynamIQ Shared Unit (DSU), creating a reasonable inference that ARM's DSU documentation also applies to the Accused Products with DynamIQ architectures including Cortex-A510, Cortex-A710, and/or Cortex-A715 cores. Qualcomm documentation likewise confirms the use of DSU and cache coherency interconnects, such as with a "Gladiator NOC," in the manner described above to facilitate communication between the clusters. *See, e.g.*:

Claim 1	Accused Products
	The *DynamIQ™ Shared Unit-110* (DSU-110) *Power Policy Units* (PPUs) control power management for the Cortex®-A510 core. A Cortex®-A510 complex supports separate gated power domains for the complex, for each core inside the complex, and for the *Vector Processing Unit* (VPU). It also supports a dedicated voltage domain for each complex, and a voltage domain for the DSU-110 DynamIQ™ cluster. Arm Cortex-A510 Core Technical Reference Manual at p. 39 When you implement a DSU-110 DynamIQ™ cluster, all interfacing between the cores, complexes, and the *DynamIQ™ Shared Unit-110* (DSU-110) is implemented automatically. All the external signal inputs and outputs pass through the DSU-110. The DSU-110 buffers and resynchronizes many of these signals to allow cores and complexes to be clocked at different speeds. The memory interfacing of each core is internally connected to the DSU-110 L3 memory system. Where necessary, the DSU-110 implements additional buffering to compensate for different clock rates of the core and DSU-110 L3 memory system. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 34 All cores in the DSU-110 DynamIQ™ cluster, including those in complexes, are coherently connected to an L3 memory system that includes an L3 cache and a *Snoop Control Unit* (SCU). The SCU maintains coherency between caches in the cores and the L3 cache, and includes a snoop filter to optimize coherency maintenance operations. The shared L3 cache simplifies process migration between the cores. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 18

Claim 1	Accused Products
	Snoop Control Unit The *Snoop Control Unit* (SCU) maintains coherency between all the data caches in the cluster. The SCU contains buffers that can handle direct cache-to-cache transfers between cores without having to read or write data to the L3 cache. Cache line migration enables dirty lines to be moved between cores. Also, there is no requirement to write back transferred cache line data to the L3 cache. The SCU contains a set of snoop filters that track the addresses for locations cached in the core caches. Including the snoop filters means that the SCU does not need to request a look up in the core caches when it receives a coherent memory request. These snoop filters are accessed by coherent requests from the other cores or from the system. If there is a simultaneous hit in the L3 tags and the SCU snoop filters, then the L3 cache normally provides the data in preference to a core. The size of the snoop filter is automatically determined from the configured number of cores and the cache sizes in those cores. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 35

Claim 1	Accused Products



Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 17

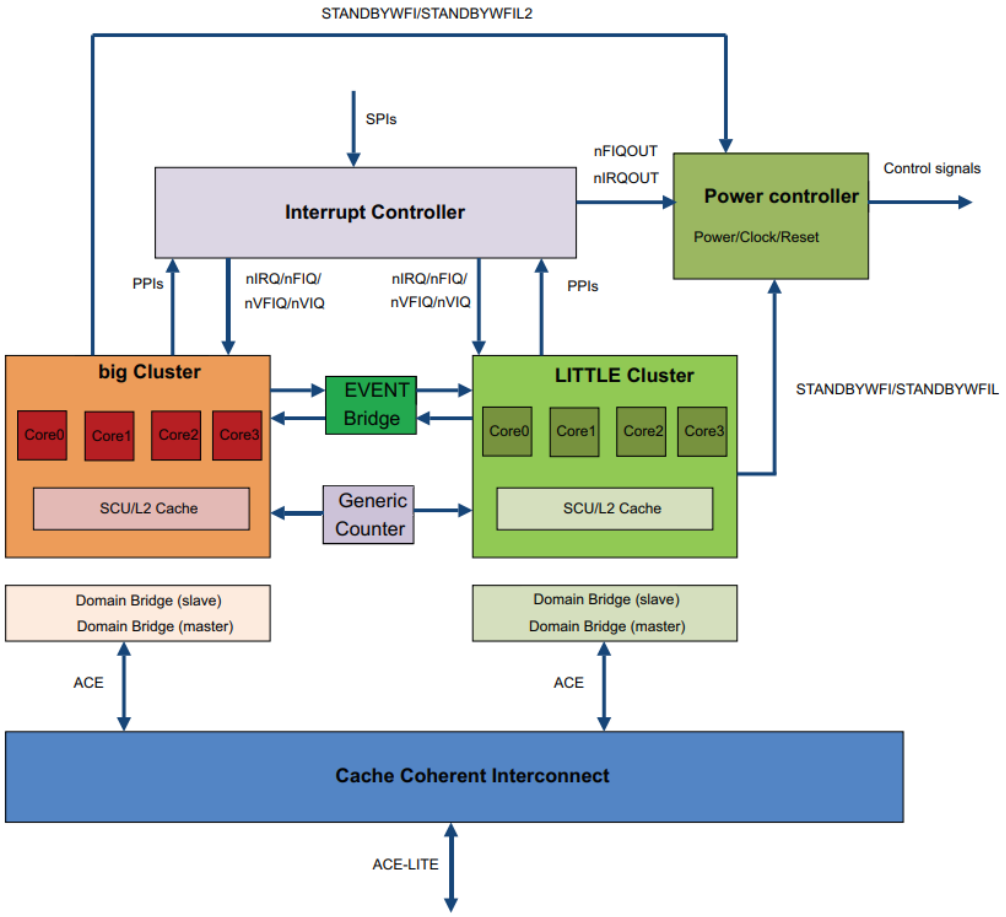
1.2 Document scope

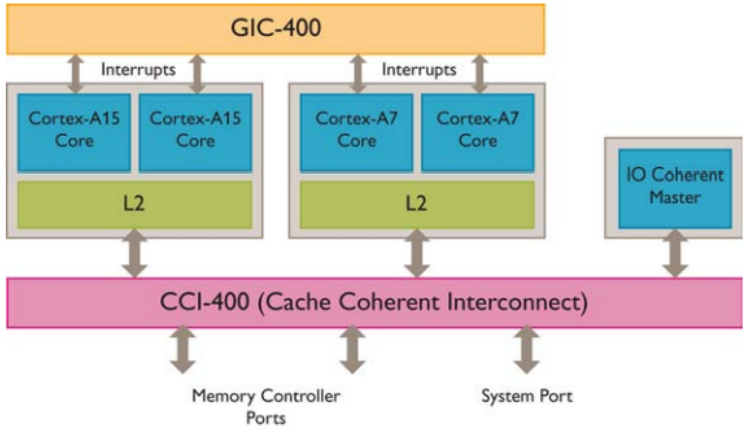
This application note focuses on the following processors and highlights important issues when powering up or powering down processor cores and clusters on an SoC.

- Cortex®-A7.
- Cortex®-A15.
- Cortex®-A17.
- Cortex®-A53.
- Cortex®-A57.
- Cortex®-A72.
- Cortex®-A73.

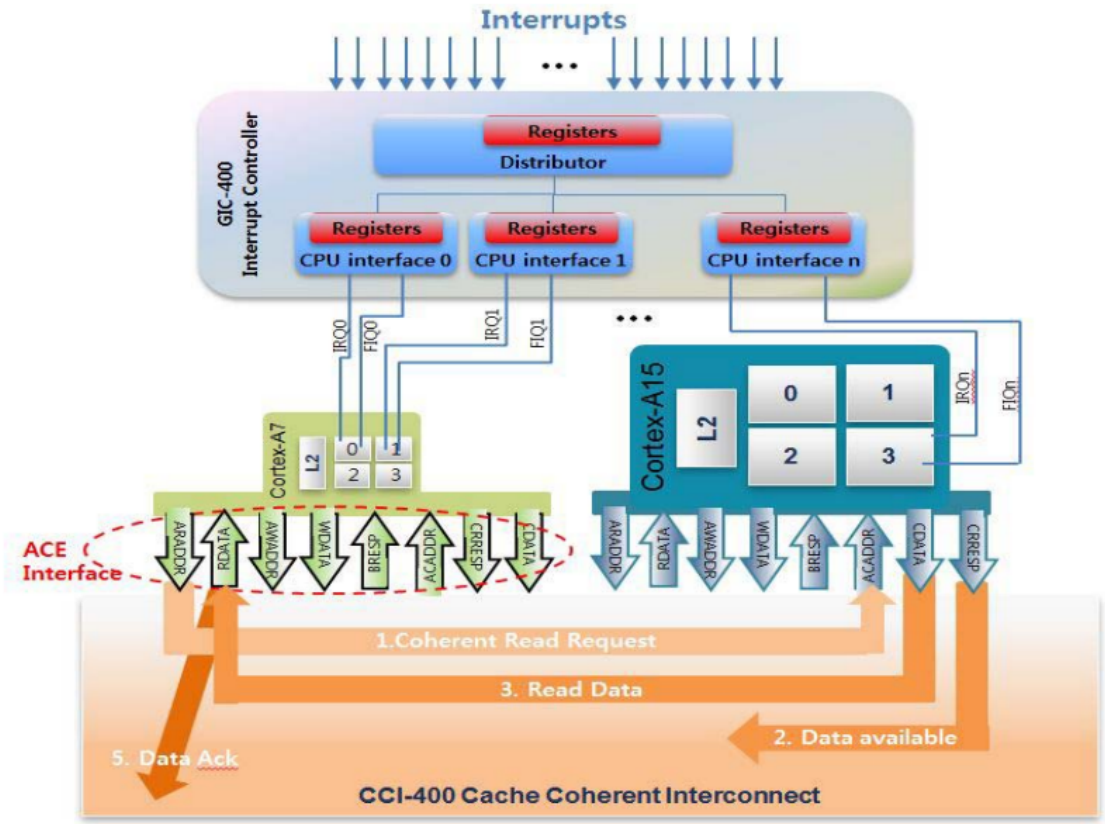
"High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products
	2.1 ARM® big.LITTLE™ system example A big.LITTLE system uses two different types of cores that are combined in a coherent system. big cores are designed for high performance while LITTLE cores are designed for high energy efficiency. The big cores are used for resource-intensive software threads, and energy-efficient LITTLE cores handle low-intensity software threads that use fewer compute resources. The result is high energy efficiency and high performance. "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products
	 **Figure 2-1 A typical big.LITTLE system** "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

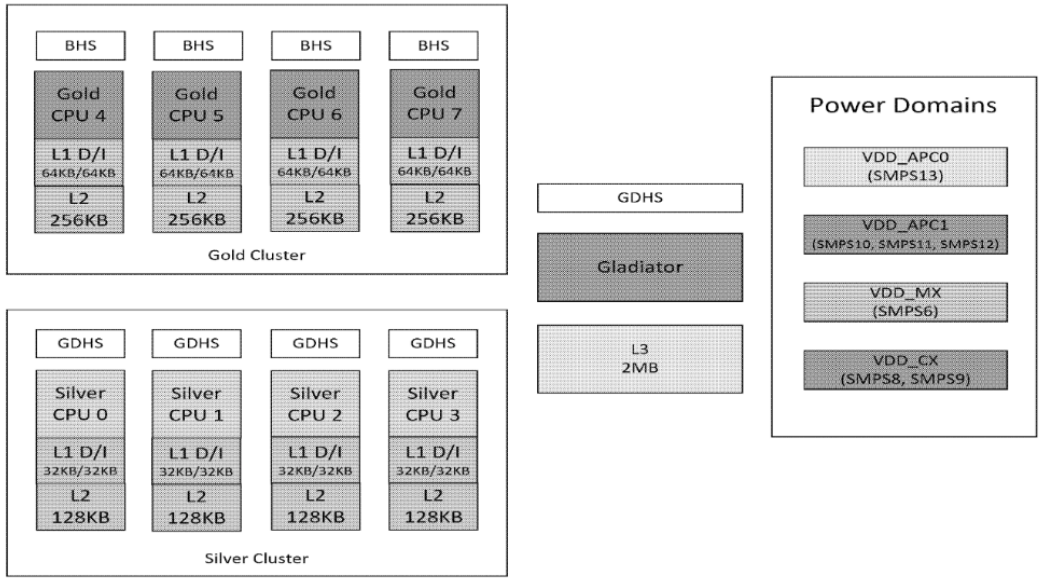
Claim 1	Accused Products
	 **Fig 1: Typical big.LITTLE system** As an example, Figure 2 describes the pipeline designs for the Cortex-A15 and Cortex-A7 cores. The Cortex-A15 core is designed to achieve high performance by running more instructions in parallel on a bigger and more complex pipeline. On the other hand, the Cortex-A7 core's pipeline is relatively simple and is designed to be extremely power efficient. The Cortex-A7 core's performance is lower than the Cortex-A15 core's but it is sufficient for most common usage scenarios executed by modern mobile devices. In fact, the Cortex-A7 core's performance is close to Cortex-A9 core, which powers most smartphones today. ARM White Paper "big.LITTLE Technology: The Future of Mobile Making very high performance available in a mobile envelope without sacrificing energy efficiency," available at https://armkeil.blob.core.windows.net/developer/Files/pdf/white-paper/big-little-technology-the-future-of-mobile.pdf

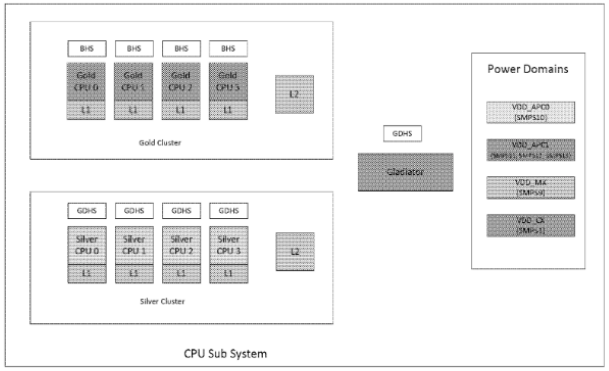
Claim 1	Accused Products
	Cache Coherency Interface and big.LITTLE Technology The key ingredient that makes big.LITTLE technology possible is coherency. big.LITTLE software models require transparent and performant transfer of data between big and LITTLE processors. Hardware coherency enables this, transparently to the software. Without hardware coherency, the transfer of data between big and LITTLE cores would always occur through main memory - this would be slow and not power efficient. In addition, it would require complex cache management software, to enable data conherency between big and LITTLE processors Figure 4 is an example of CPU subsystem consisting of a Cortex-A7 cluster, a Cortex-A15 cluster and a set of system fabric components which enable the seamless data transfer between clusters. This fabric is collectively referred to as a "Cache Coherent Interconnect" – in this case the ARM CoreLink™ CCI-400 interconnect IP. The system is completed by the CoreLink GIC-400, which provides dynamically configurable interrupt distribution to all the cores. ARM White Paper "big.LITTLE Technology: The Future of Mobile Making very high performance available in a mobile envelope without sacrificing energy efficiency," available at https://armkeil.blob.core.windows.net/developer/Files/pdf/white-paper/big-little-technology-the-future-of-mobile.pdf

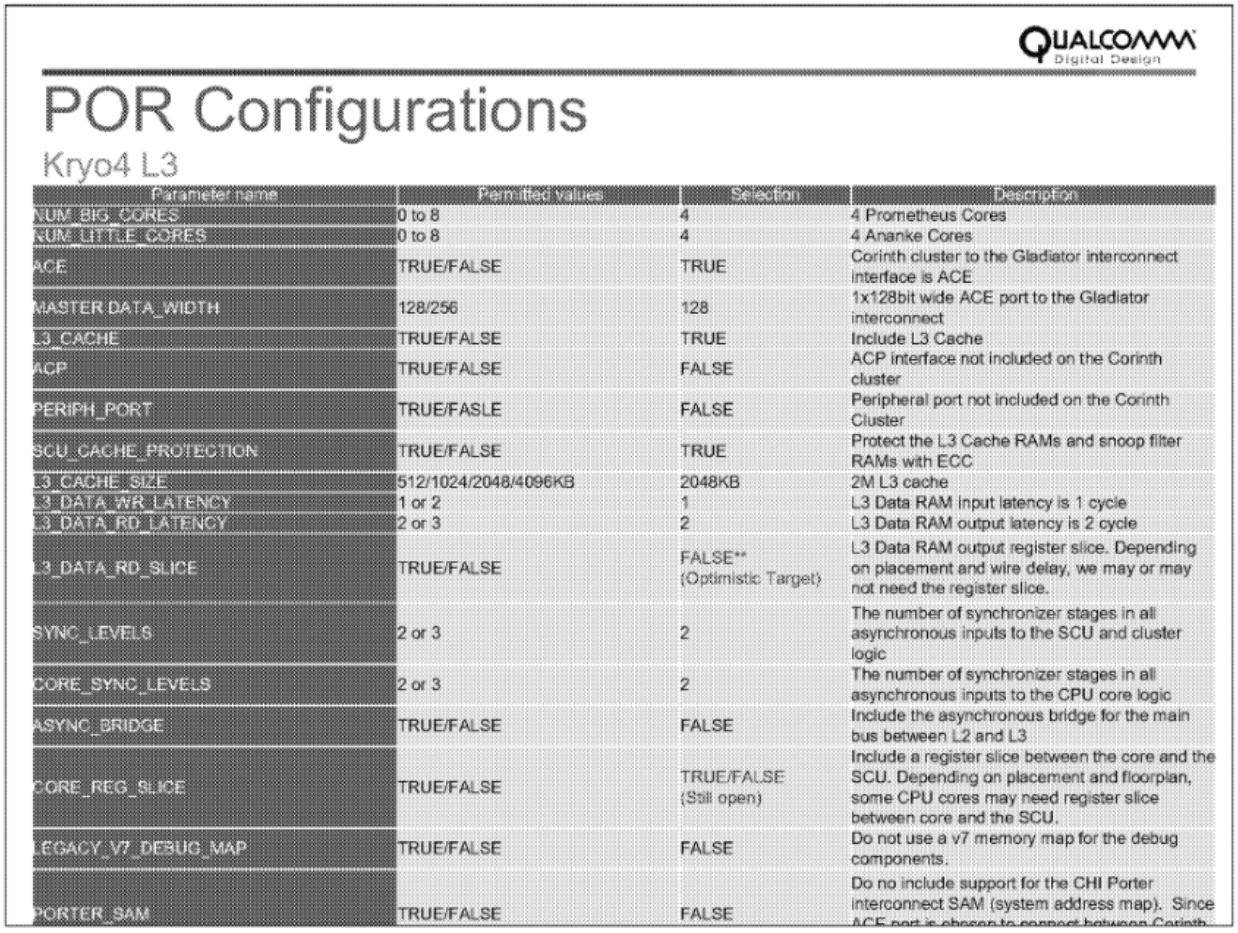
Claim 1	Accused Products
	 **Figure 3: Cache coherency in a big.LITTLE system** ARM White Paper "big.LITTLE Technology: The Future of Mobile Making very high performance available in a mobile envelope without sacrificing energy efficiency," available at https://armkeil.blob.core.windows.net/developer/Files/pdf/white-paper/big-little-technology-the-future-of-mobile.pdf

Claim 1	Accused Products

	As shown in Figure 3, the bus interfaces of Cortex-A15 and Cortex-A7 processors make use of the AMBA® AXI Coherency Extensions (ACE) to the widely-used AMBA AXI protocol. This protocol provides for coherent data transfer at the bus level. In the AMBA ACE protocol, three coherency channels are added in addition to the normal five channels of AMBA AXI. As an example, the lower part of Figure shows the steps in a coherent data read from the Cortex-A7 cluster to the Cortex-A15 cluster. This starts with the Cortex-A7 cluster issuing a Coherent Read Request through the RADDR channel. The CCI-400 hands over the request to the Cortex-A15 processor's ACADDR channel to snoop into Cortex-A15 processor's cache. On receiving the request from CCI-400, the Cortex-A15 processor checks the data availability and reports this information back through the CRRESP channel. If the requested data is in the cache, the Cortex-A15 processor places it on the CDATA channel. Then the CCI-400 moves the data from the Cortex-A15 processor's CDATA channel to the Cortex-A7 processor's RDATA channel, resulting in a cache linefill in the Cortex-A7 processor. The CCI-400 and the ACE protocol enable full coherency between the Cortex-A15 and Cortex-A7 clusters, allowing data sharing to take place without external memory transactions.
	
	ARM White Paper "big.LITTLE Technology: The Future of Mobile Making very high performance available in a mobile envelope without sacrificing energy efficiency," available at https://armkeil.blob.core.windows.net/developer/Files/pdf/white-paper/big-little-technology-the-future-of-mobile.pdf
	
	Gladiator NOC
	
	▪ Gladiator NOC provides interconnect – Cache Coherency Interconnect (CCI) between:
	  ▪ Kryo clusters
	  ▪ DDR
	  ▪ System Network Operations Center (NOC)
	▪ Gladiator clock control handled in RPM
	  ▪ In MSM8996, kernel manages the CCI clocks
	▪ Provides hang detection and error reporting
	
	QCREDSTONE_0082759 at -72.

Claim 1	Accused Products
	CPU Subsystem (cont.)  QCREDSTONE_0036560 at -71

Claim 1	Accused Products
	CPU Power ▪ Customized 64-bit ARM v8-compliant apps processor (Kryo 2xx CPU) ▪ Two Clusters in CPU subsystem – Kryo Gold and Kryo Silver ▪ Kryo Gold Cluster – Quad Kryo high performance CPUs with 2.5 GHz to 2.7 GHz Speed ▪ Kryo Silver Cluster – Quad Kryo low power CPUs with 1.5 GHz to 1.9 GHz Speed ▪ L1 and L2 Cache: ▪ L2 cache at 2 MB for Kryo Gold ▪ L2 cache at 1 MB for Kryo Silver ▪ Power rails: ▪ Kryo Gold cluster and Silver cluster have dedicated, separate power rails ▪ PM8998 SMPS10 powers the Kryo Silver cluster ▪ PM8998 SMPS11/12/13 are tied together as a single trace to power the Kryo Gold cluster ▪ Each Kryo Gold core has a block head switch (BHS) and each Kryo Silver core has a global distributed head switch (GDHS) to power the core ▪ Gold and Silver cluster, along with the respective L2 cache, can operate on a different clock source at different frequencies. ▪ Within a cluster, the cores and L2 are synchronous  QCREDSTONE_0082868 at-78.

Claim 1	Accused Products
	 QCREDSTONE_0087481 at -93.

QUALCOMM Digital Design

POR Configurations

Kryo4 L3

Parameter name	Permitted values	Selection	Description
NUM_BIG_CORES	0 to 8	4	4 Prometheus Cores
NUM_LITTLE_CORES	0 to 8	4	4 Ananke Cores
ACE	TRUE/FALSE	TRUE	Corinth cluster to the Gladiator interconnect interface is ACE
MASTER DATA_WIDTH	128/256	128	1x128bit wide ACE port to the Gladiator interconnect
L3_CACHE	TRUE/FALSE	TRUE	Include L3 Cache
ACP	TRUE/FALSE	FALSE	ACP interface not included on the Corinth cluster
PERIPH_PORT	TRUE/FASLE	FALSE	Peripheral port not included on the Corinth Cluster
SCU_CACHE_PROTECTION	TRUE/FALSE	TRUE	Protect the L3 Cache RAMs and snoop filter RAMs with ECC
L3_CACHE_SIZE	512/1024/2048/4096KB	2048KB	2M L3 cache
L3_DATA_WR_LATENCY	1 or 2	1	L3 Data RAM input latency is 1 cycle
L3_DATA_RD_LATENCY	2 or 3	2	L3 Data RAM output latency is 2 cycle
L3_DATA_RD_SLICE	TRUE/FALSE	FALSE** (Optimistic Target)	L3 Data RAM output register slice. Depending on placement and wire delay, we may or may not need the register slice.
SYNC_LEVELS	2 or 3	2	The number of synchronizer stages in all asynchronous inputs to the SCU and cluster logic
CORE_SYNC_LEVELS	2 or 3	2	The number of synchronizer stages in all asynchronous inputs to the CPU core logic
ASYNC_BRIDGE	TRUE/FALSE	FALSE	Include the asynchronous bridge for the main bus between L2 and L3
CORE_REG_SLICE	TRUE/FALSE	TRUE/FALSE (Still open)	Include a register slice between the core and the SCU. Depending on placement and floorplan, some CPU cores may need register slice between core and the SCU.
LEGACY_V7_DEBUG_MAP	TRUE/FALSE	FALSE	Do not use a v7 memory map for the debug components.
PORTER_SAM	TRUE/FALSE	FALSE	Do no include support for the CHI Porter interconnect SAM (system address map). Since ACE port is chosen to connect between Corinth

Claim 1	Accused Products
	1.2 Features This section provides a summary of features of the CPU SS subsystem. ▪ Hard macro consisting of quad core CMaiaA53 CPU performance cluster and quad core CA53 CPU power cluster (These cores are ARM's implementation of the ARMv8 architecture). ▪ CA53 CPU Power Cluster 0 optimized for power with 32 kB I/D L1 cache, 512 kB L2 cache. ECC/Parity cache protection supported for both L1 and L2. ▪ CMaiaA53 CPU Performance Cluster 1 optimized for performance with 48 kB I, 32 KB D L1 cache, 1 MB L2 cache. ECC/Parity cache protection supported for both L1 and L2. ▪ CA53 cores in both power and performance cluster optimized for symmetric PPA (Power, Performance and Area). ▪ Cache Coherent Interconnect (Gladiator) connecting two CPU clusters using ACE interfaces and interfacing with memory sub System with two interleaved AXI3 compliant interfaces. Gladiator S13 port connects to the power cluster and S24 port connects to the performance cluster. Gladiator S03 port is for the Gladiator register accesses from APSS AHB. Gladiator M1 , M2 port is core for memory and device accesses. QCREDSTONE_0087836 at -39.

Claim 1	Accused Products

8 Kryo Clocks and Resets

8.1 Clocks:

The DSU requires clock signals for each of the cores, internal logic, and external interfaces. The following table describes the clocks.

Signal	Description
CORECLK[CN:0]	The per-core clocks for all core logic including L1 caches and L2 caches.
SCLK	The clock for the SCU and L3 memory system, including the ACE or CHI master interface. **SCLK** is also used for any cores that are configured to run synchronously to the DSU.
PCLK	The clock for the DebugBlock and DSU debug APB interfaces. **Note:** The DebugBlock and cluster both have **PCLK** inputs. You might choose to connect these to the same clock. Alternatively, you might choose to place an asynchronous bridge between the two clock inputs, in which case they might be different clocks.
ATCLK	The clock for the ATB trace buses output from the DSU. **Note :** All ATB buses output from the DSU share the same clock.
GICCLK	The clock for the GIC AXI-stream interface between the DSU and an external GIC
PERIPHCLK	The clock for peripheral logic inside the DSU such as timers, and clock and power management logic.

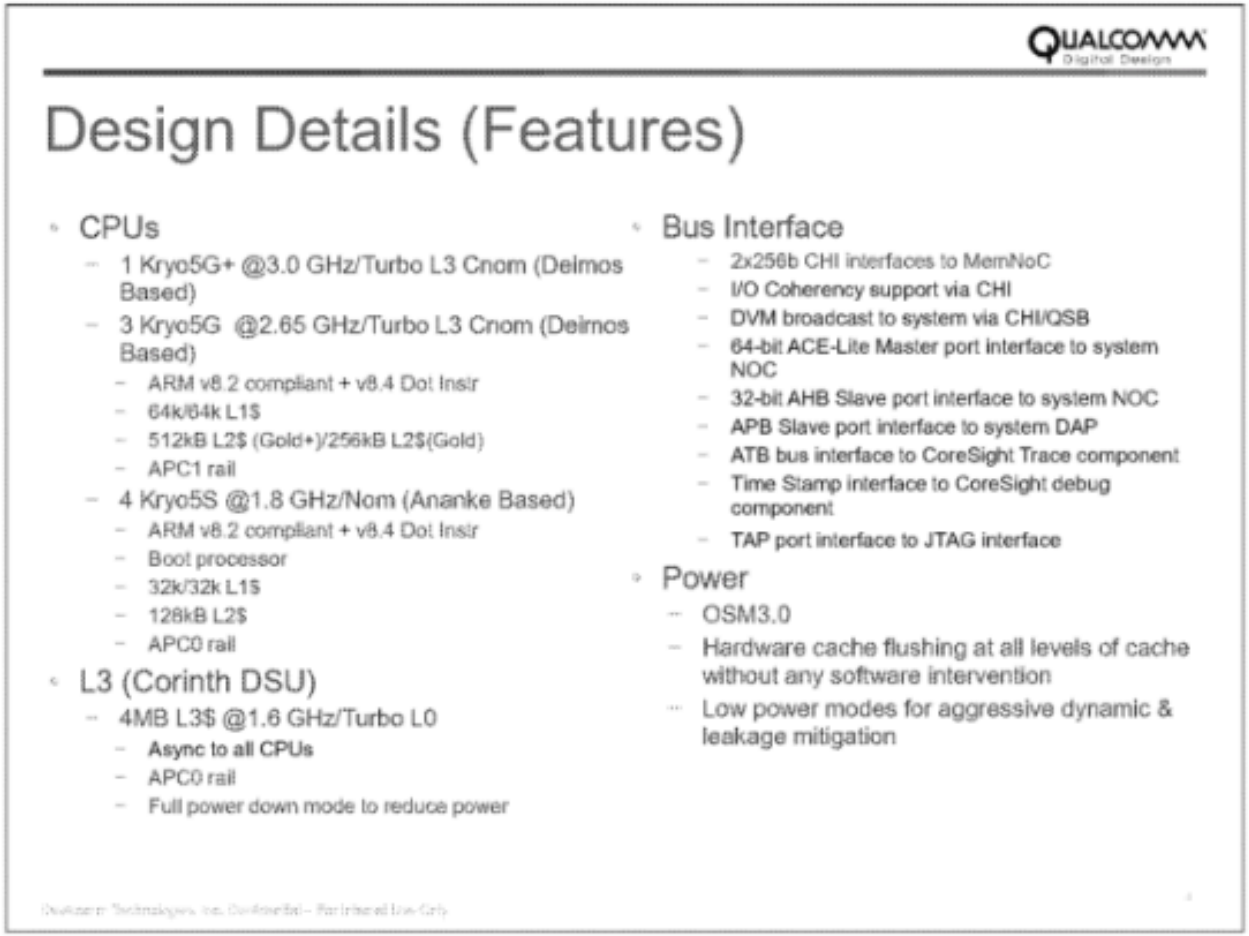
All clocks can be driven fully asynchronously to each other. The DSU contains all the necessary synchronizing logic for crossing between clock domains. There are no clock dividers and no latches in the design. The entire design is rising edge triggered.

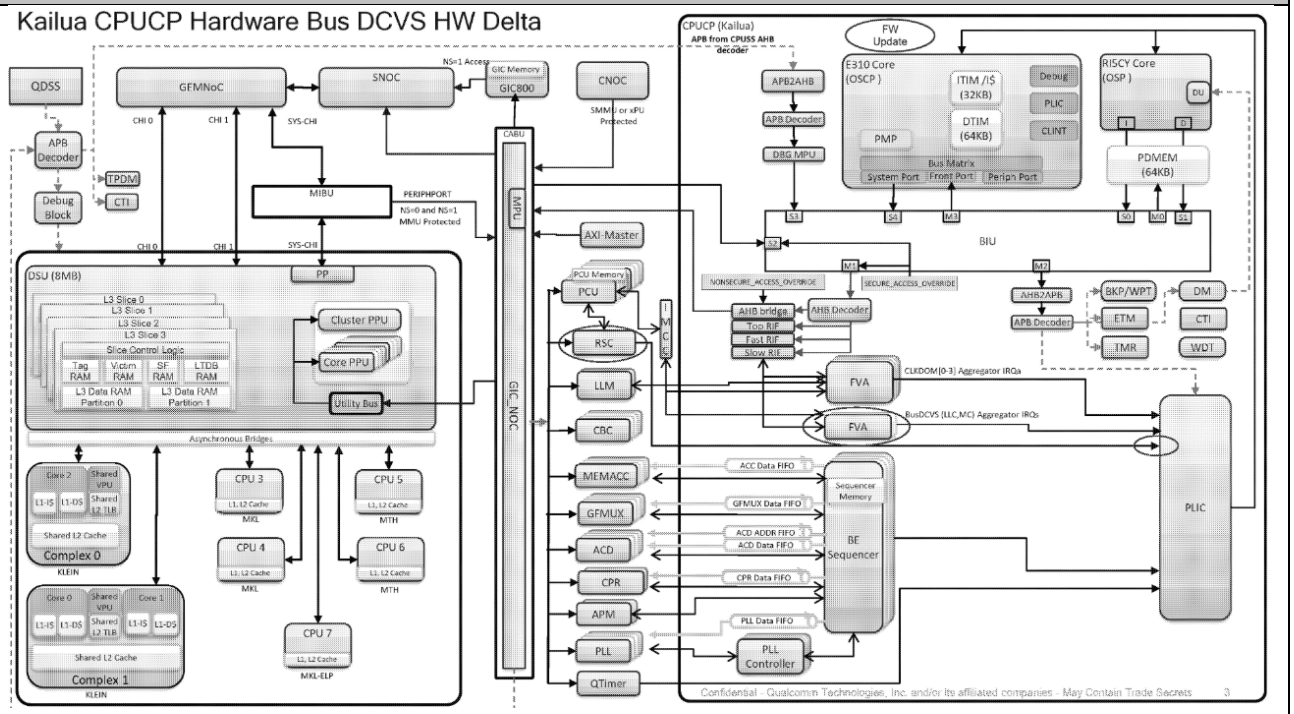
Note :

- It is possible to configure some or all the cores to run synchronously with the L3 memory system. If this option is chosen, the corresponding **CORECLK** signals are not present and the synchronous cores run with **SCLK**.
- The DebugBlock can be clocked by a different clock from the DSU **PCLK**. To allow this, the macrocell implementer can choose to add asynchronous bridges between the DSU and the DebugBlock.

Some external interfaces, such as the main ACE or CHI master interface, support a clock enable input to

QCREDSTONE _0088972 at -91.

Claim 1	Accused Products
	 QCREDSTONE_0089100 at -04.

Claim 1	Accused Products
	 QCREDSTONE_0098768 at -70.

Claim 1	Accused Products

6 Kryo Clocks and Resets

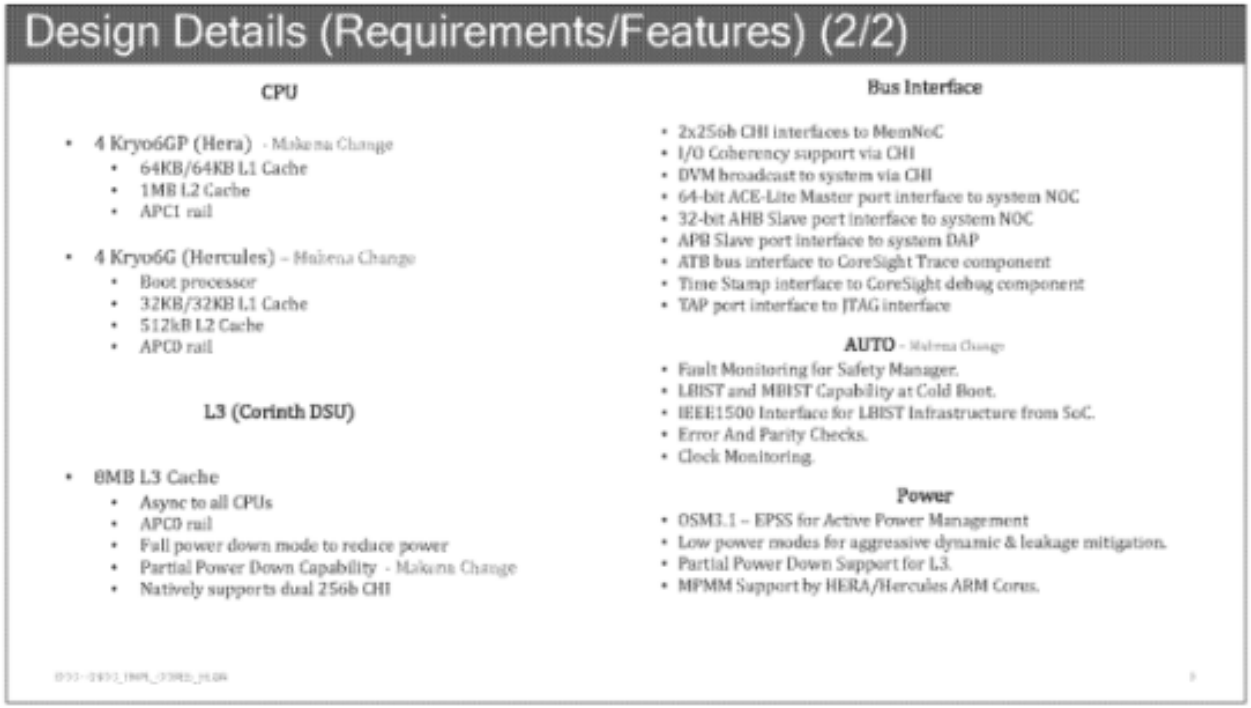
6.1 Clocks:

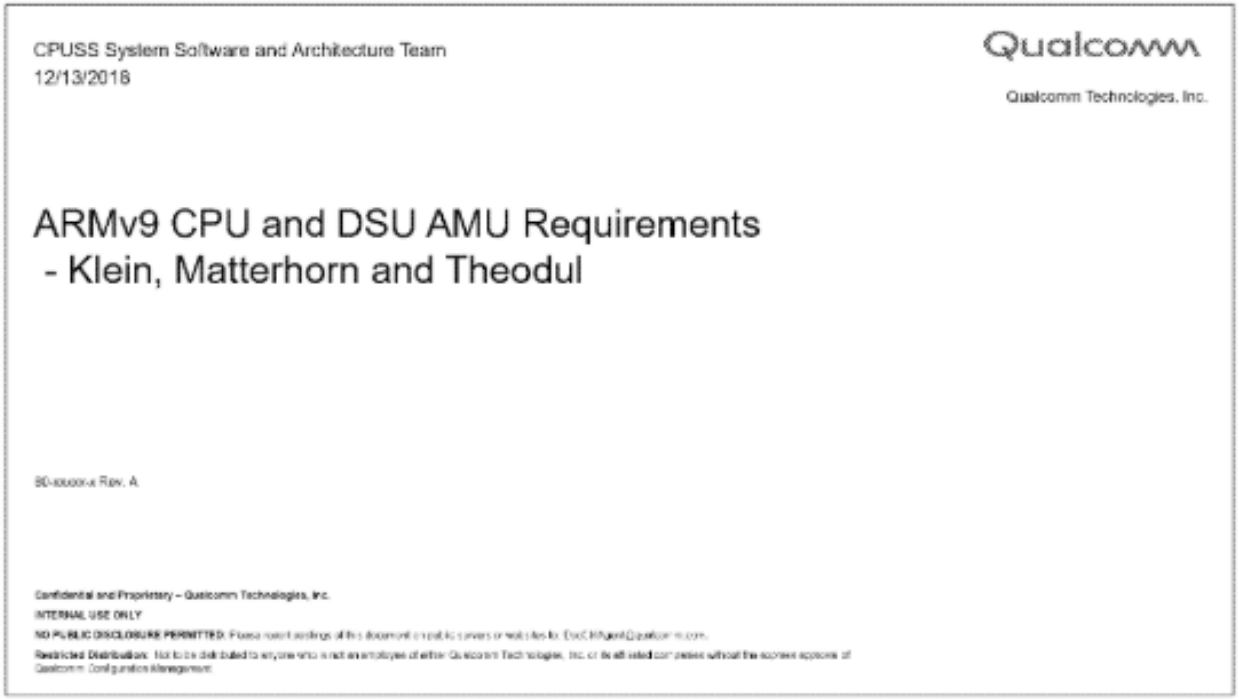
The DSU requires clock signals for each of the cores, internal logic, and external interfaces. The following table describes the clocks.

Signal	Description
CORECLK[CN:0]	The per-core clocks for all core logic including L1 caches and L2 caches.
SCLK	The clock for the SCU and L3 memory system, including the ACE or CHI master interface. **SCLK** is also used for any cores that are configured to run synchronously to the DSU.
PCLK	The clock for the DebugBlock and DSU debug APB interfaces.
	Note: The DebugBlock and cluster both have **PCLK** inputs. You might choose to connect these to the same clock. Alternatively, you might choose to place an asynchronous bridge between the two clock inputs, in which case they might be different clocks.
ATCLK	The clock for the ATB trace buses output from the DSU. **Note :** All ATB buses output from the DSU share the same clock.
GICCLK	The clock for the GIC AXI-stream interface between the DSU and an external GIC
PERIPHCLK	The clock for peripheral logic inside the DSU such as timers, and clock and power management logic.

All clocks can be driven fully asynchronously to each other. The DSU contains all the necessary synchronizing logic for crossing between clock domains. There are no clock dividers and no latches in the design. The entire design is rising edge triggered.

QCREDSTONE_0090274 at -91, -92.

Claim 1	Accused Products
	 QCREDSTONE_0091858 at -66.

Claim 1	Accused Products
	 QCREDSTONE_0098363.

Claim 5

Claim 5	Accused Products
5. The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one	Each Accused Product comprises a multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a periphery of the multi-core processor. For example, according to ARM's documents and reference design, the multi-core processor should contain a system control processor (SCP) to control voltage, power, and clocks, and power policy units (PPUs) to manage power states on each voltage domain. On information and belief,

Claim 5	Accused Products
or more control blocks located in a periphery of the multi-core processor.	each DynamIQ Accused Product contains an SCP and one or more PPUs as described. Identification of the physical location of the control blocks is proprietary information of Qualcomm that is the proper subject of fact discovery and to date no production detailing the physical location of any blocks has been made. For another example, according to ARM's documents and reference design, a big.LITTLE multi-core processor should contain a power controller and other controllers for supplying control signals as claimed. Identification of the physical location of the control blocks is proprietary information of Qualcomm that is the proper subject of fact discovery and to date no production detailing the physical location of any such blocks has been made. *See, e.g.*:

Claim 5	Accused Products

6.1 The Power Policy Unit

Power mode control for the *DynamIQ™ Shared Unit-110* (DSU-110) is provided by the *Power Policy Units* (PPUs) that are integrated into the cluster. These PPUs control all the PPU modes for all components in the cluster.

A PPU is a standard component for abstracting software-controlled power domain policy to low-level hardware control signaling. There is one PPU for controlling the DSU-110 DynamIQ™ cluster power domain (PDCLUSTER). Also, each core has its own individual PPU for controlling its respective core power domain (for example, a PPU for PDCORE0 and a PPU for PDCORE1). This includes any cores included as part of a complex.

A component in the system such as a *System Control Processor* (SCP) can program the PPUs through the utility bus to set the required power policy. The PPUs control the low-level details of powering up, powering down, and resetting domains as necessary to implement the requested policy. The hardware performs any actions to reach the requested power mode, such as gating clocks, cleaning and invalidating caches, or disabling coherency.



- Although the cluster and each core in the cluster has their own PPU, the shared logic of a complex does not have a dedicated PPU. Instead, power management of the complex is controlled as a combination of the PPUs for the cores it contains. See Table 5-8: PPU mode and power domain states for a dual-core complex on page 74.
- The cluster and all the core PPUs are provided as part of the DSU-110.
- The implementation process automatically creates the PPU for the cluster and each core PPU, and connects these into the DSU-110 DynamIQ™ cluster. Each PPU has a set of memory-mapped control registers which is accessed using the utility bus.

Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 78

Claim 5	Accused Products
	4.3 Power control Good power management is key to reduce system power consumption while maintaining a high performance. An RD-TC21 reference subsystem contains the following power management features: • Multiple voltage domains to allow for *Dynamic Voltage and Frequency Scaling* (DVFS) on application processors and the GPU • Multiple power-gated regions provide comprehensive leakage management • Multiple power modes for different system scenarios • A *System Control Processor* (SCP) based on a Cortex®-M3 processor controls power, clock, reset, and the static configuration of the system • *Power Policy Units* (PPUs) are used to manage power states of each voltage and power domain under the control of the SCP Arm® Total Compute 2021 Reference Design Software Developer Guide at 47-48

Claim 5	Accused Products
	SCP runtime firmware The SCP runtime firmware executes after *Trusted Firmware for A-profile* (TF-A) BL2 has authenticated and copied it from flash. The SCP runtime firmware performs the following functions: • Responds to *System Control and Management Interface* (SCMI) messages through *Message Handling Unit* (MHU) version 2.0 for processor power control and *Dynamic Voltage and Frequency Scaling* (DVFS) • Power domain management • Clock management *Id.* at p. 65

Claim 5	Accused Products

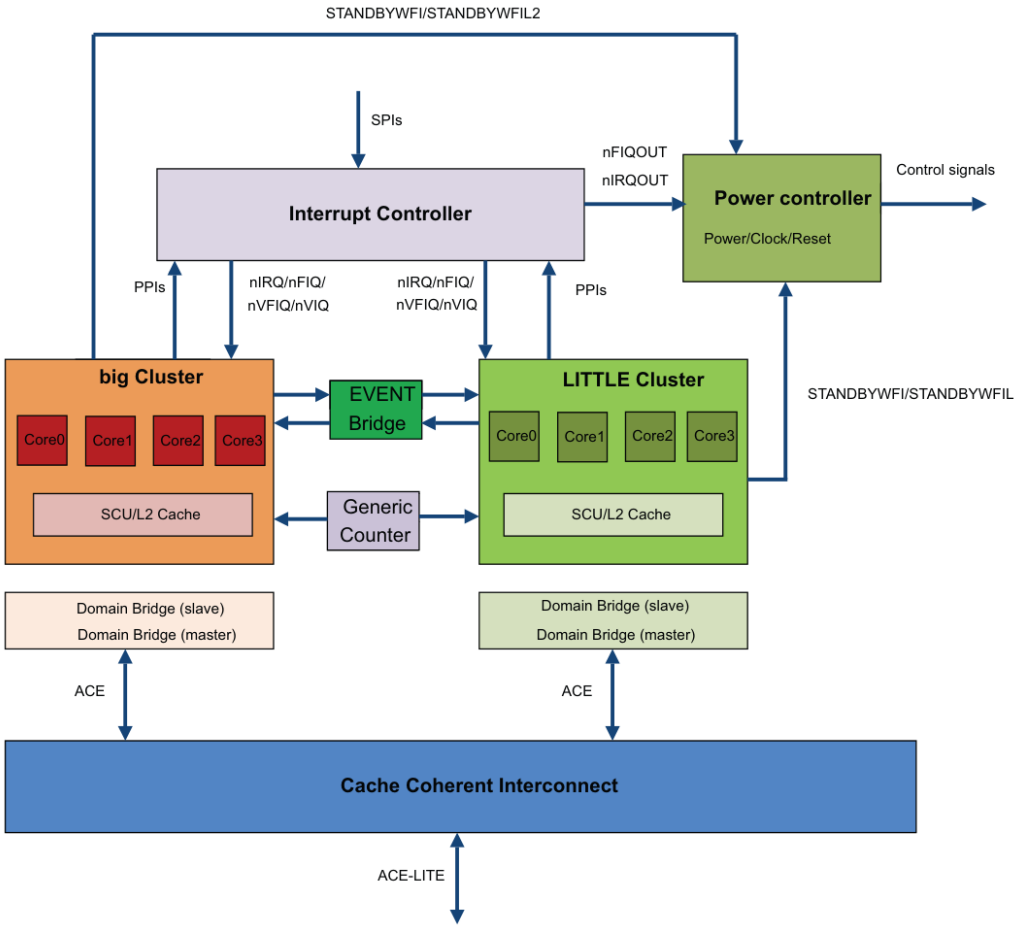
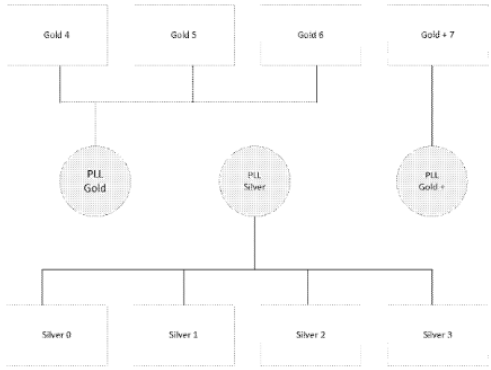
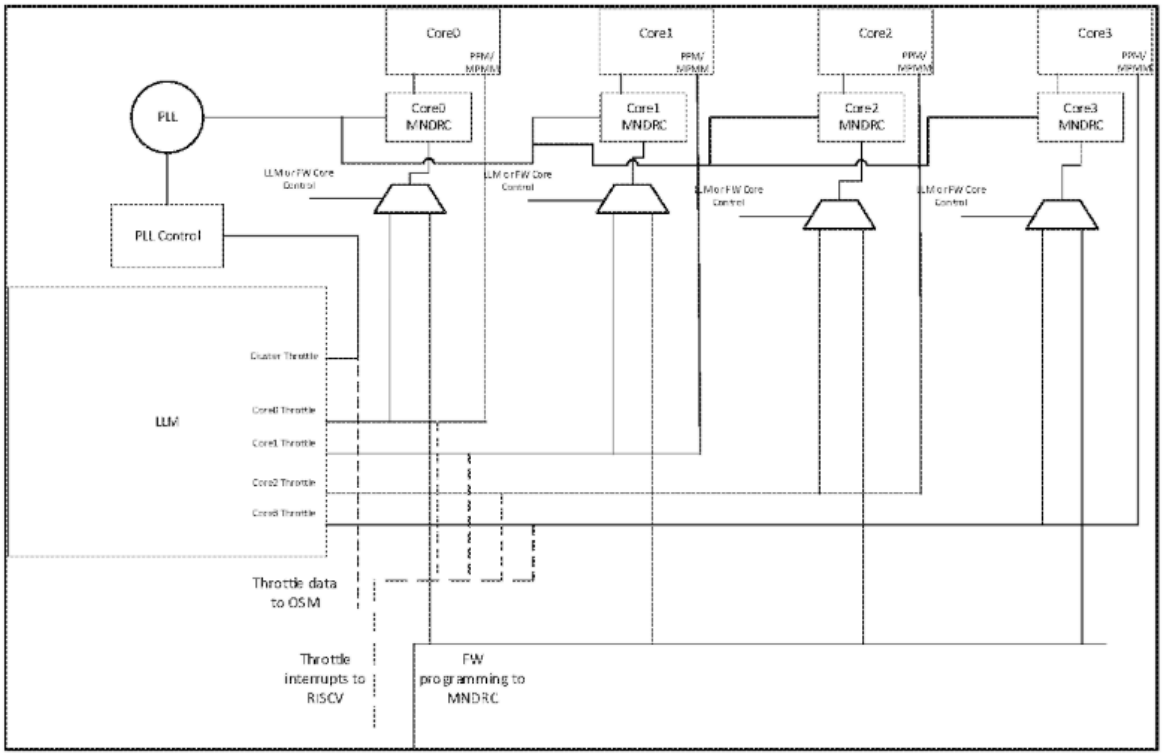


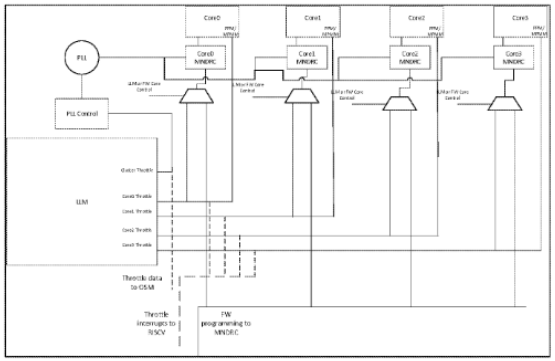
Figure 2-1 A typical big.LITTLE system

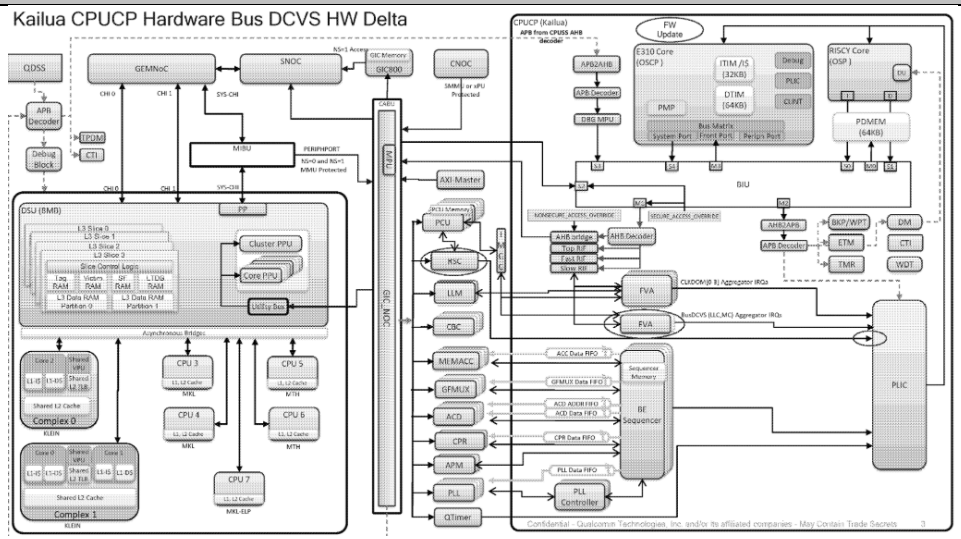
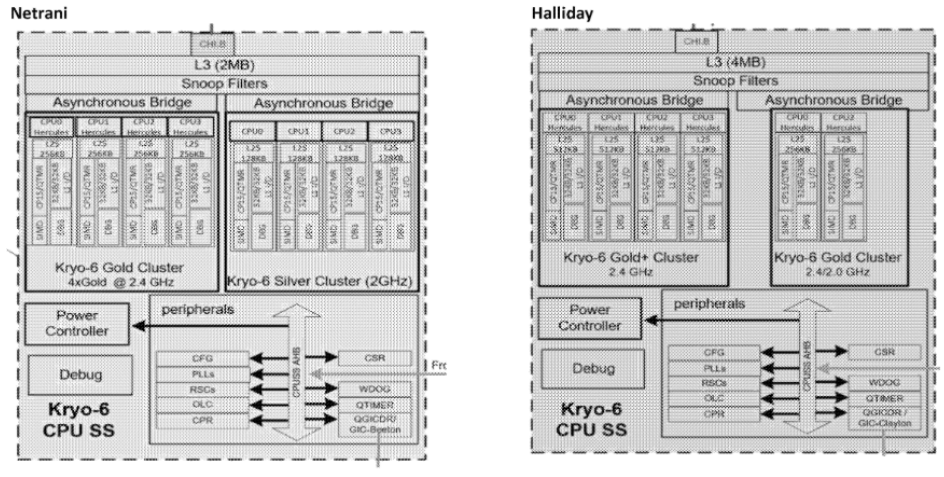
"High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/, at 15 (2-3)

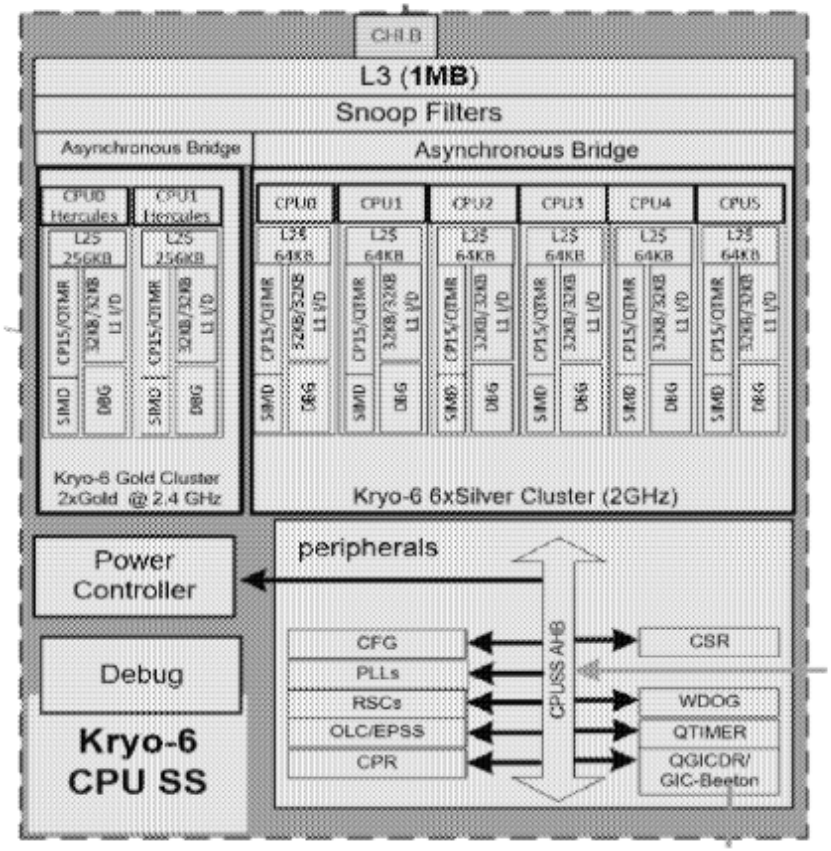
Claim 5	Accused Products
	2.1.1 big cluster and LITTLE cluster This example system uses a big cluster and a LITTLE cluster, and each cluster consists of four cores. There are five power domains for each cluster. Each core is in its own power domain to enable individual powerdown. The rest of the logic within a cluster is in a different power domain. Isolation cells exist between power domains for isolation. Each cluster is implemented in an independent voltage domain with an independent clock source. Each of the clusters has a unique Dynamic Voltage and Frequency Scaling (DVFS) curve. Therefore, cores in the same cluster must traverse an *Operating Performance Point* (OPP) together. You can change the OPP of cores in a cluster, without affecting the cores in the other cluster. *Id.* **2.1.2 Power controller** The power controller contains the hardware power control functions of the SoC. The operations of the power controller are both directed by the *Operating System Power Management* (OSPM) software and hardware events in the system. The power controller works closely with relevant signals of ARM IPs and other system components for power saving. *Id.* Qualcomm's documentation confirms the accused products include the same or similar SCP, PPU, and Power Controller blocks.

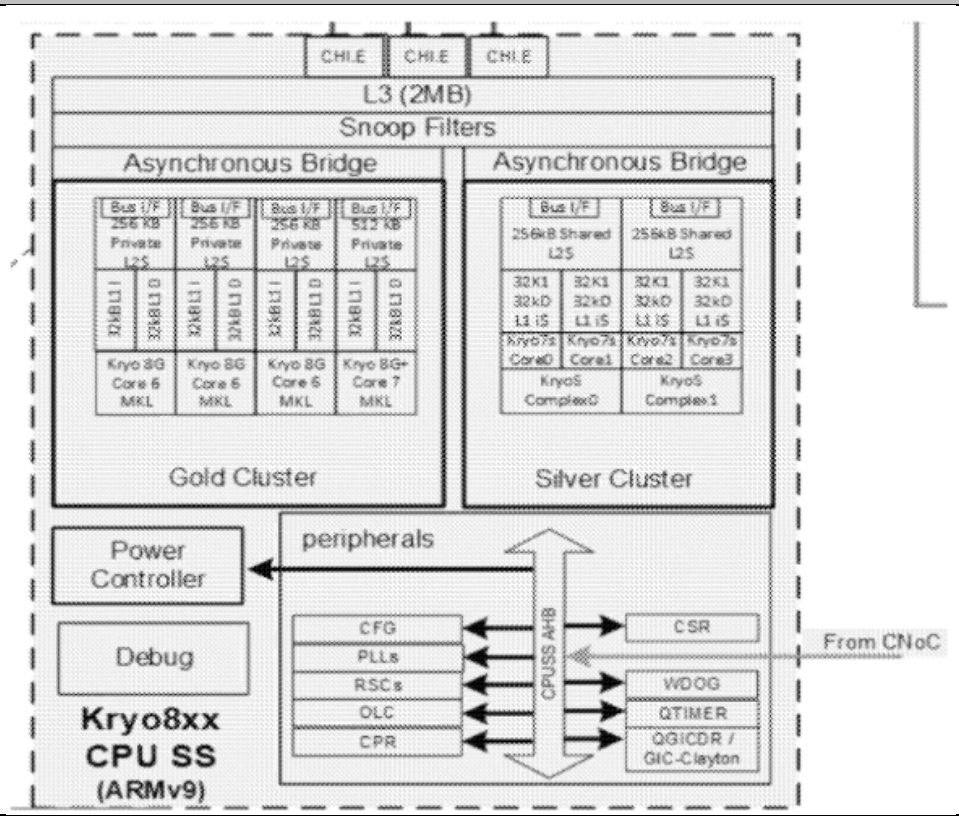
Claim 5	Accused Products
	Motivation Current implementation • Current implementation in CPUSS requires that each core per cluster domain run at the same clock frequency. • This requirement is due to the fact that each core doesn't have its own PLL. • OSM aggregates and chooses MAX frequency for operation for those cores. 

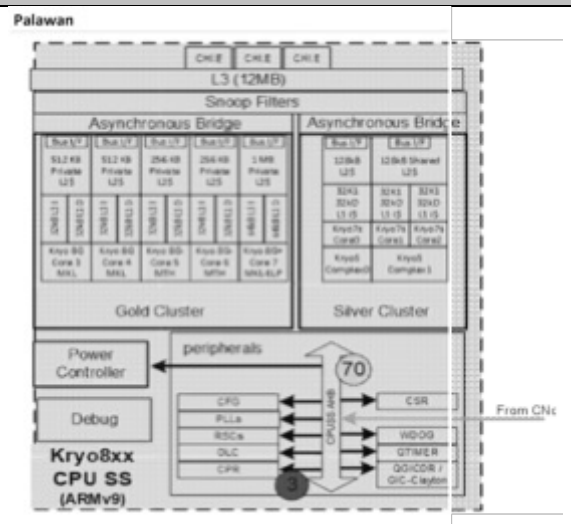
Claim 5	Accused Products
	 Kailua

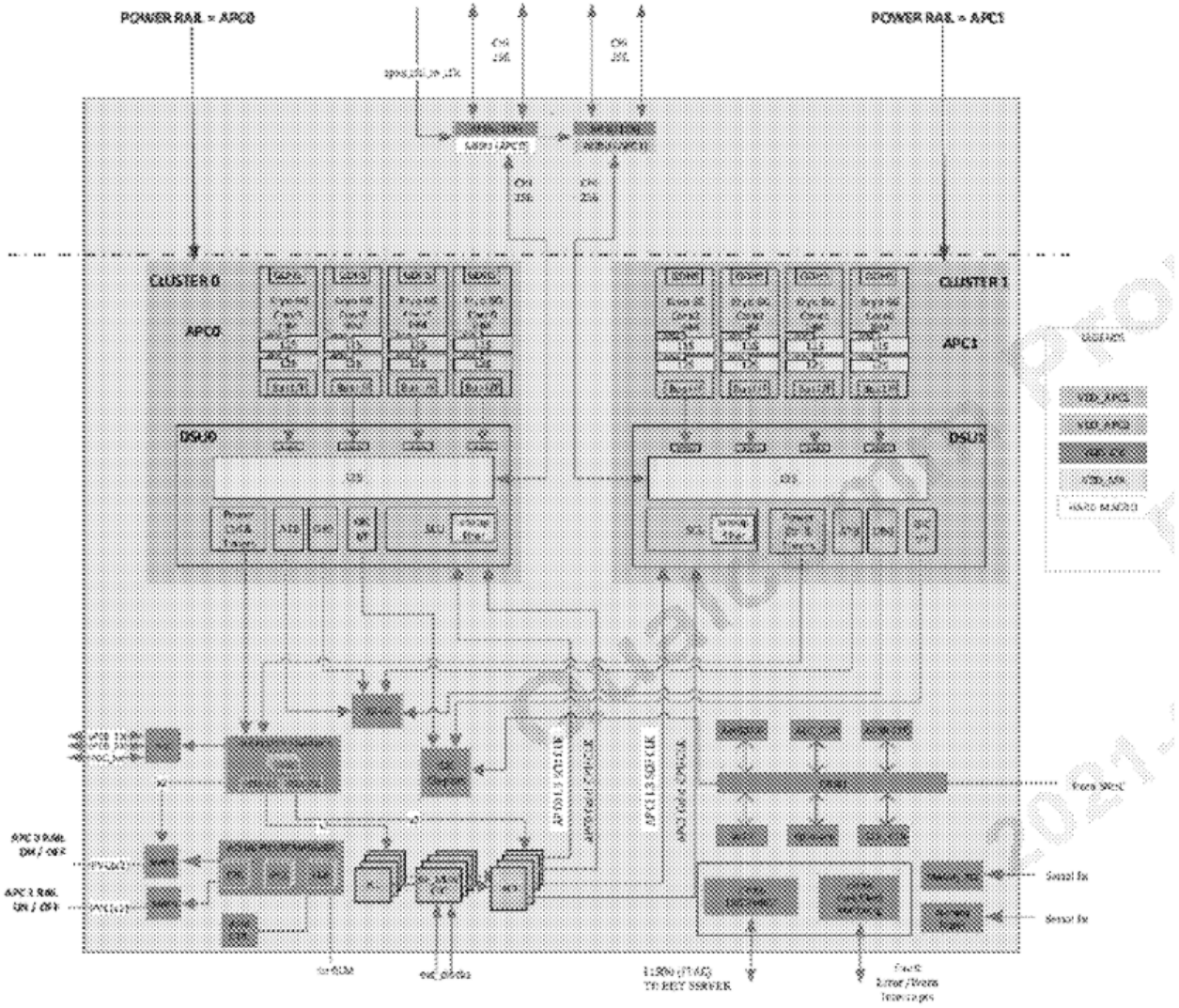
Claim 5	Accused Products
	LLM & FW Interaction • For Kailua implementation the MNDRC's can either be controlled by FW or by LLM directly but not by both. • When testing for LLM thermal mitigation data the MUX control is switched to LLM that will drive per core MVAL based on it's LUT table. • When gathering power profile data for SW the MUX control is switched to FW. • Note that if there is a need to capture data from SW and LLM driven MVAL's to MNDRC then Interrupt driven control is to be used to ensure we have single master that drives MVAL. • Note that POR implementation for inner and outer loop and per core MPMM/PPM control remains the same. • The Design has been introduced such that it does not affect POR requirements of LLM and FW Source sample text 15  QCREDSTONE_0098870 at -74, -83, -84.

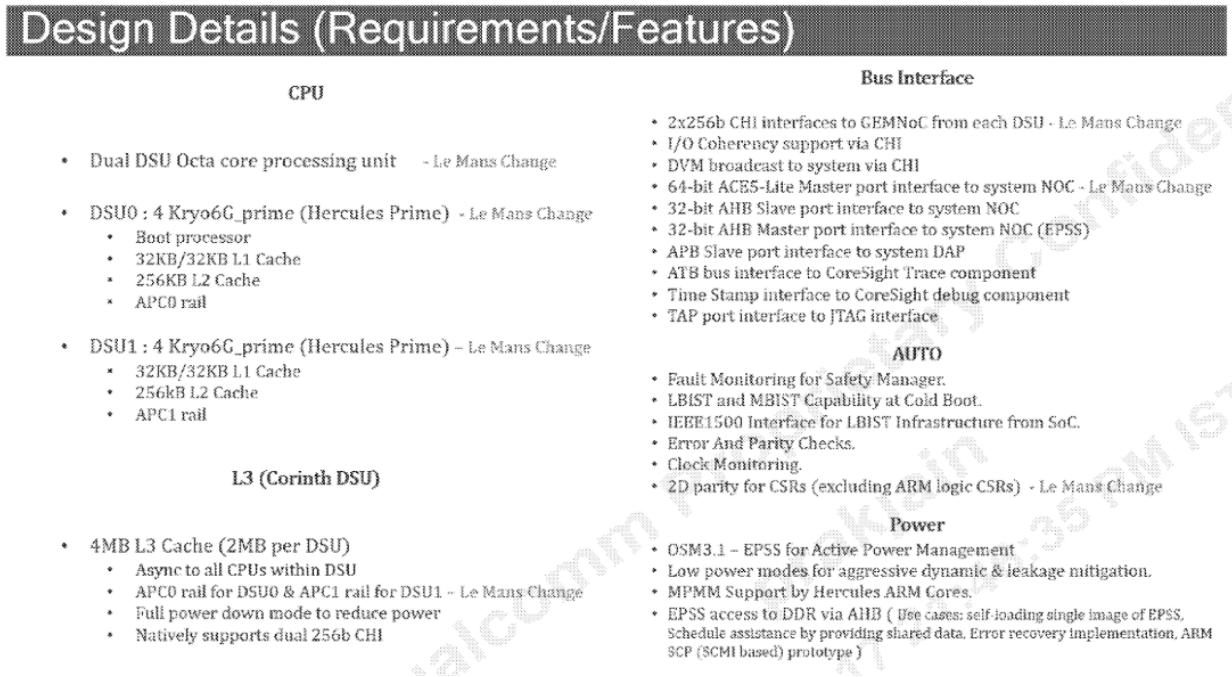
Claim 5	Accused Products
	 QCREDSTONE_0098768 at -70. 

Claim 5	Accused Products
	Clarence 

Claim 5	Accused Products
	

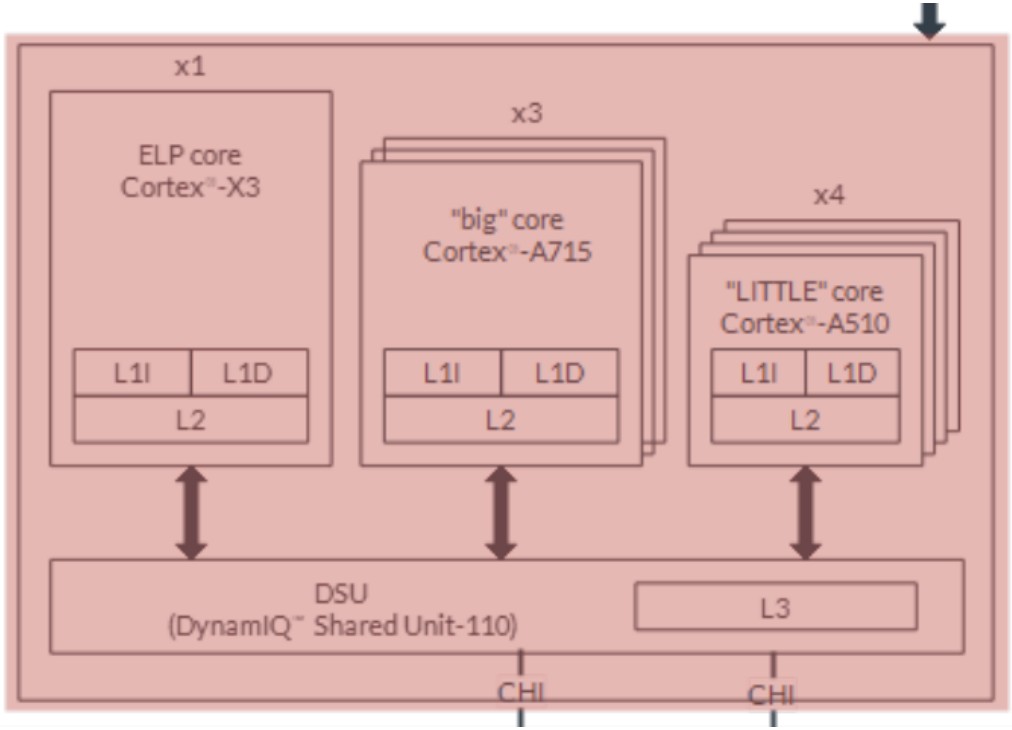
Claim 5	Accused Products
	 QCREDSTONE_0098556 at -558 to -562.

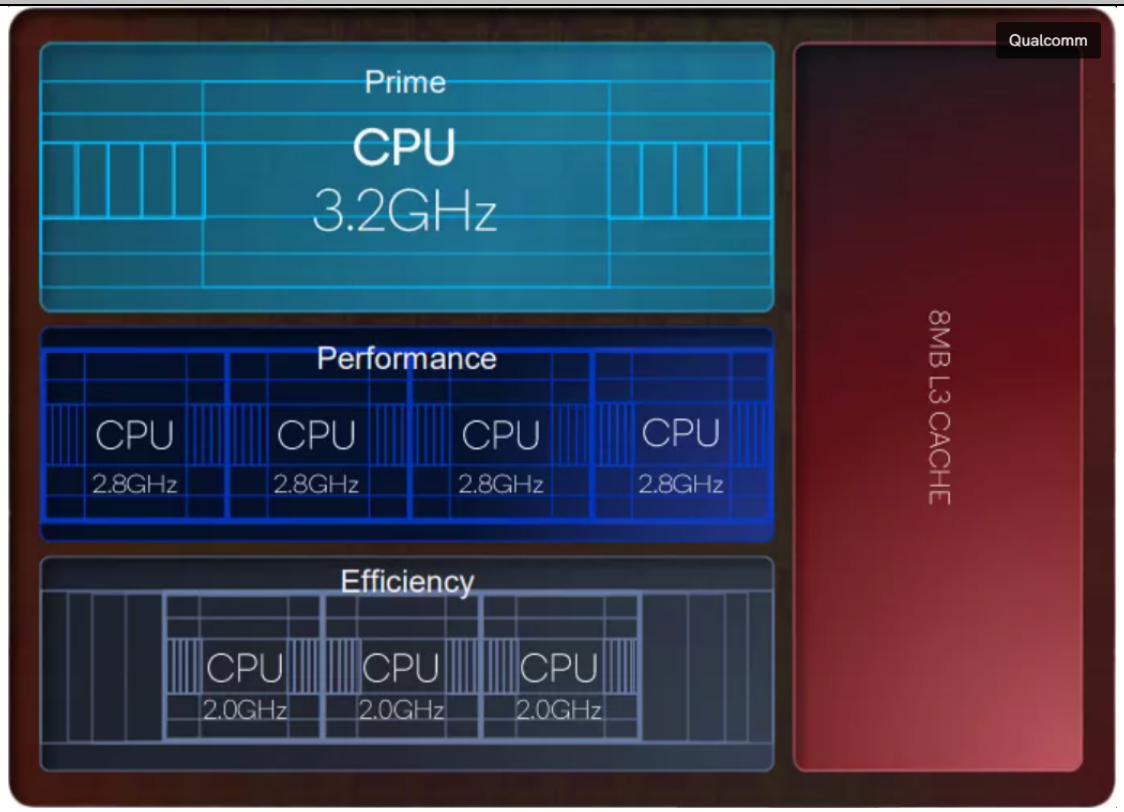
Claim 5	Accused Products
	

Claim 5	Accused Products
	 QCREDSTONE_0091177 at -86-87.

Claim 8

Claim 8	Accused Products
8. The multi-core processor of claim 1, wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located	Each Accused Product comprises a multi-core processor of claim 1, wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor. For example, on information and belief each core is located a region of the multi-core processor. Identification of the physical arrangement of the cores is proprietary information of Qualcomm

Claim 8	Accused Products
in a second region of the multi-core processor.	that is the proper subject of fact discovery and to date no production detailing the physical location of any blocks has been made. *See, e.g.*:  Arm® Total Compute 2021 Reference Design Software Developer Guide at 15

Claim 8	Accused Products
	 https://www.androidauthority.com/snapdragon-8-gen-2-explained-3231826/

Claim 8	Accused Products

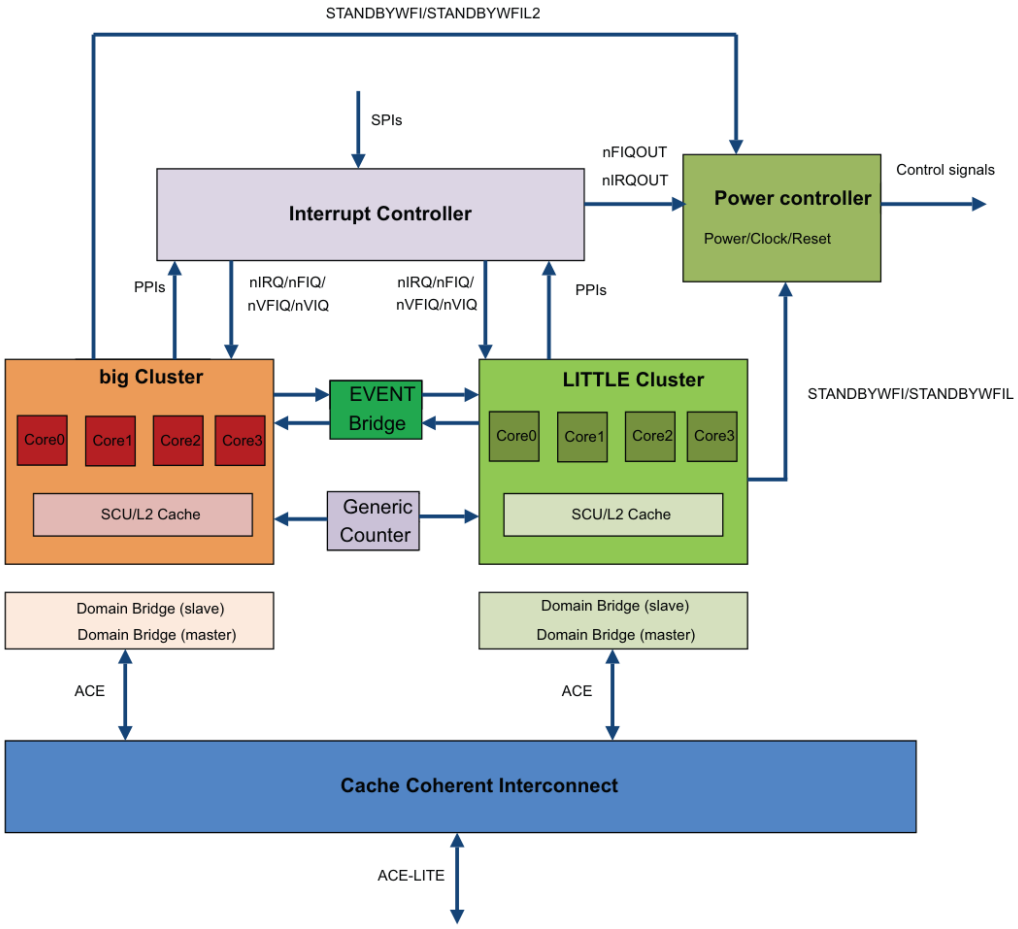


Figure 2-1 A typical big.LITTLE system

"High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/, at 15 (2-3)

Claim 8	Accused Products
	On information and belief, Qualcomm physically groups components, including groups of processor cores based on common voltages/power such groups of processor cores such as the first and second processor cores are each physically grouped together as they use voltage APC0 and APC1 respectively, *see e.g.* QCREDSTONE_0091177 at -87, -87, QCREDSTONE_0096091 at -104:

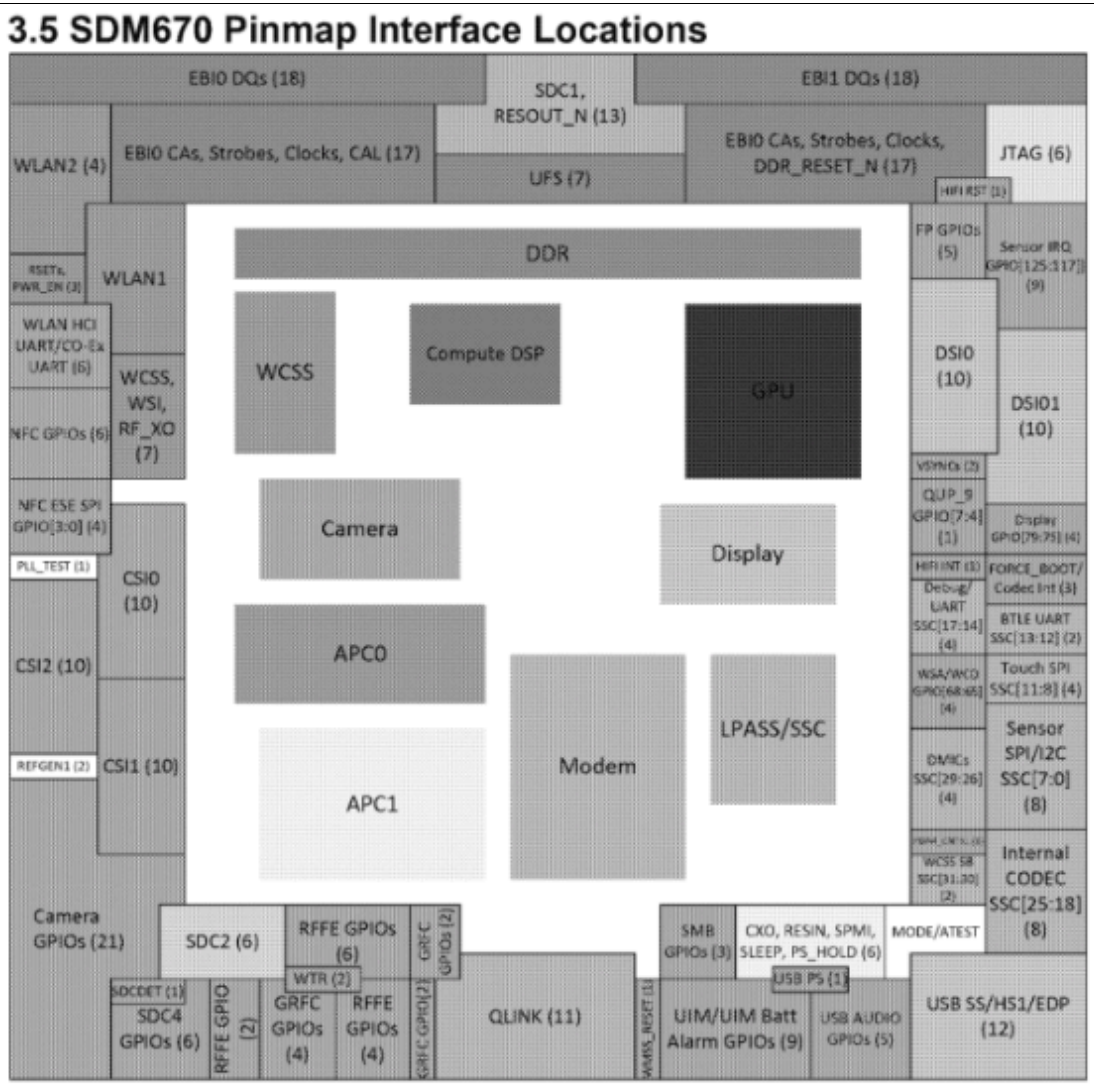


Figure 3-4 SDM670 Pinmap interface signal and IO assignment diagram

QCREDSTONE_0031600 at -21.

Claim 9

Claim 9	Accused Products
9. The multi-core processor of claim 8, wherein the first region and the second region are overlapping regions of the multi-core processor.	Each Accused Product comprises a multi-core processor of claim 8, wherein the first region and the second region are overlapping regions of the multi-core processor. For example, on information and belief there is either some overlap or no overlap of the first and second regions. Identification of the physical arrangement of the cores is proprietary information of Qualcomm that is the proper subject of fact discovery and to date no production detailing the physical location of any blocks has been made.

Claim 10

Claim 10	Accused Products
10. The multi-core processor of claim 8, wherein the first region and the second region are non-overlapping regions of the multi-core processor.	Each Accused Product comprises a multi-core processor of claim 8, wherein the first region and the second region are non-overlapping regions of the multi-core processor. For example, on information and belief there is either some overlap or no overlap of the first and second regions. Identification of the physical arrangement of the cores is proprietary information of Qualcomm that is the proper subject of fact discovery and to date no production detailing the physical location of any blocks has been made. On information and belief, Qualcomm physically groups components, including groups of processor cores based on common voltages/power such groups of processor cores such as the first and second processor cores are each physically grouped together as they are in power domain APC0 and APC1 respectively, *see e.g.* QCREDSTONE_0091177 at -87, -87, QCREDSTONE_0096091 at -104:

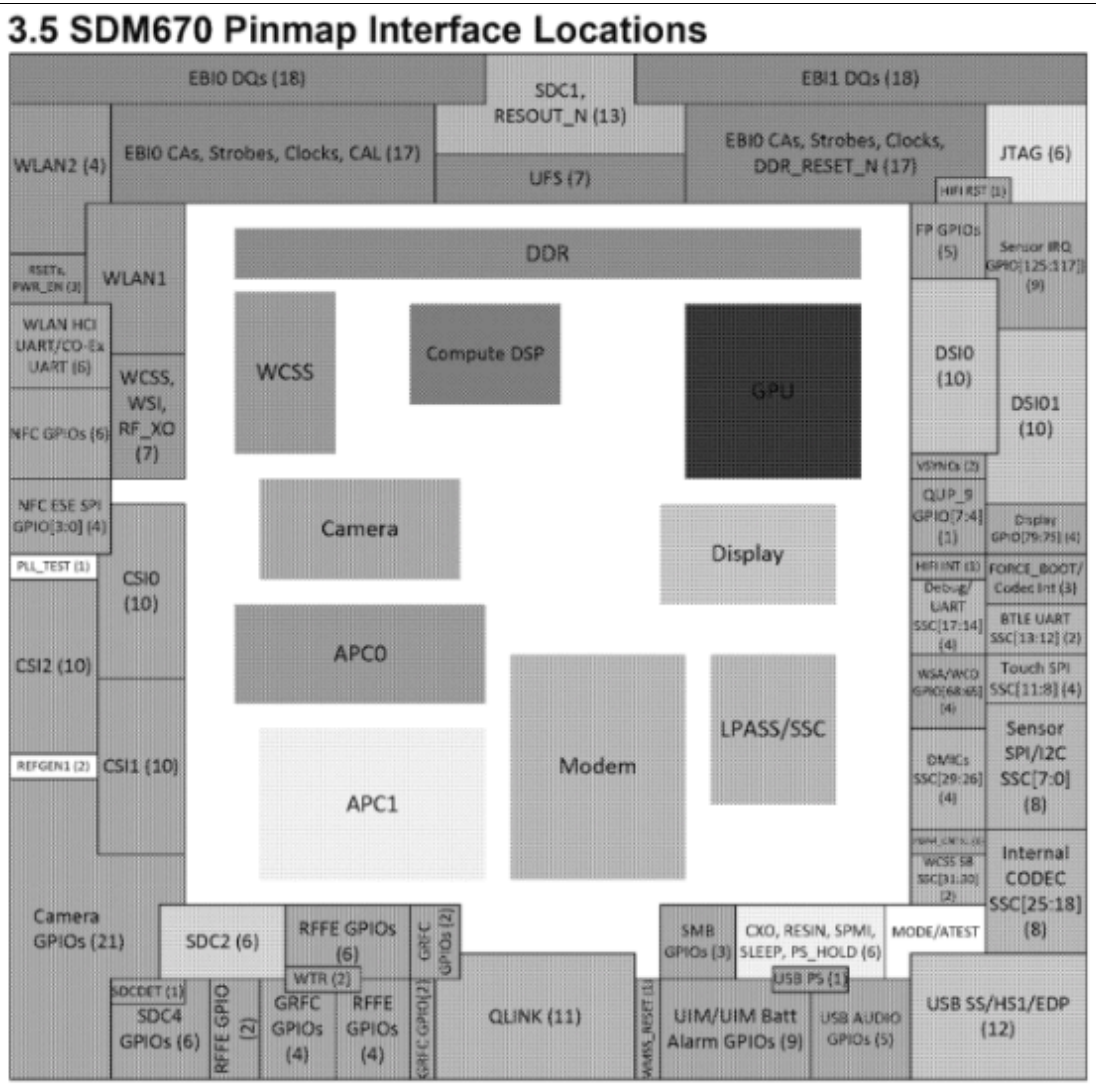


Figure 3-4 SDM670 Pinmap interface signal and IO assignment diagram

QCREDSTONE_0031600 at -21.

Claim 21

Claim 21	Accused Products
[21pre]. A multi-core processor, comprising:	To the extent the preamble is limiting, each Accused Product comprises a multi-core processor. *See* analysis and evidence of claim 1 preamble above.
[21a] a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage from a power control block and a first output clock signal from a first phase lock loop (PLL) having a first clock signal as input in a clock control block;	Each Accused Product comprises a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage from a power control block and a first output clock signal from a first phase lock loop (PLL) having a first clock signal as input in a clock control block. *See* analysis and evidence of claim element [1a] above. Furthermore, each DynamIQ Accused Product includes a power control block and a clock control block. For example, according to ARM's documents and reference design, the multi-core processor should contain a system control processor (SCP) to control voltage, power, and clocks, and power policy units (PPUs) to manage power states on each voltage domain. On information and belief, the processor in each DynamIQ Accused Product contains an SCP and one or more PPUs as described. For another example, according to ARM's documents and reference design, a big.LITTLE multi-core processor should contain a power controller and other controllers for supplying the voltage and clock signals as claimed. *See, e.g.*:

Claim 21	Accused Products

6.1 The Power Policy Unit

Power mode control for the *DynamIQ™ Shared Unit-110* (DSU-110) is provided by the *Power Policy Units* (PPUs) that are integrated into the cluster. These PPUs control all the PPU modes for all components in the cluster.

A PPU is a standard component for abstracting software-controlled power domain policy to low-level hardware control signaling. There is one PPU for controlling the DSU-110 DynamIQ™ cluster power domain (PDCLUSTER). Also, each core has its own individual PPU for controlling its respective core power domain (for example, a PPU for PDCORE0 and a PPU for PDCORE1). This includes any cores included as part of a complex.

A component in the system such as a *System Control Processor* (SCP) can program the PPUs through the utility bus to set the required power policy. The PPUs control the low-level details of powering up, powering down, and resetting domains as necessary to implement the requested policy. The hardware performs any actions to reach the requested power mode, such as gating clocks, cleaning and invalidating caches, or disabling coherency.



- Although the cluster and each core in the cluster has their own PPU, the shared logic of a complex does not have a dedicated PPU. Instead, power management of the complex is controlled as a combination of the PPUs for the cores it contains. See Table 5-8: PPU mode and power domain states for a dual-core complex on page 74.
- The cluster and all the core PPUs are provided as part of the DSU-110.
- The implementation process automatically creates the PPU for the cluster and each core PPU, and connects these into the DSU-110 DynamIQ™ cluster. Each PPU has a set of memory-mapped control registers which is accessed using the utility bus.

Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 78

Claim 21	Accused Products
	4.3 Power control Good power management is key to reduce system power consumption while maintaining a high performance. An RD-TC21 reference subsystem contains the following power management features: • Multiple voltage domains to allow for *Dynamic Voltage and Frequency Scaling* (DVFS) on application processors and the GPU • Multiple power-gated regions provide comprehensive leakage management • Multiple power modes for different system scenarios • A *System Control Processor* (SCP) based on a Cortex®-M3 processor controls power, clock, reset, and the static configuration of the system • *Power Policy Units* (PPUs) are used to manage power states of each voltage and power domain under the control of the SCP Arm® Total Compute 2021 Reference Design Software Developer Guide at 47-48

Claim 21	Accused Products
	SCP runtime firmware The SCP runtime firmware executes after *Trusted Firmware for A-profile* (TF-A) BL2 has authenticated and copied it from flash. The SCP runtime firmware performs the following functions: • Responds to *System Control and Management Interface* (SCMI) messages through *Message Handling Unit* (MHU) version 2.0 for processor power control and *Dynamic Voltage and Frequency Scaling* (DVFS) • Power domain management • Clock management *Id.* at p. 65

Claim 21	Accused Products

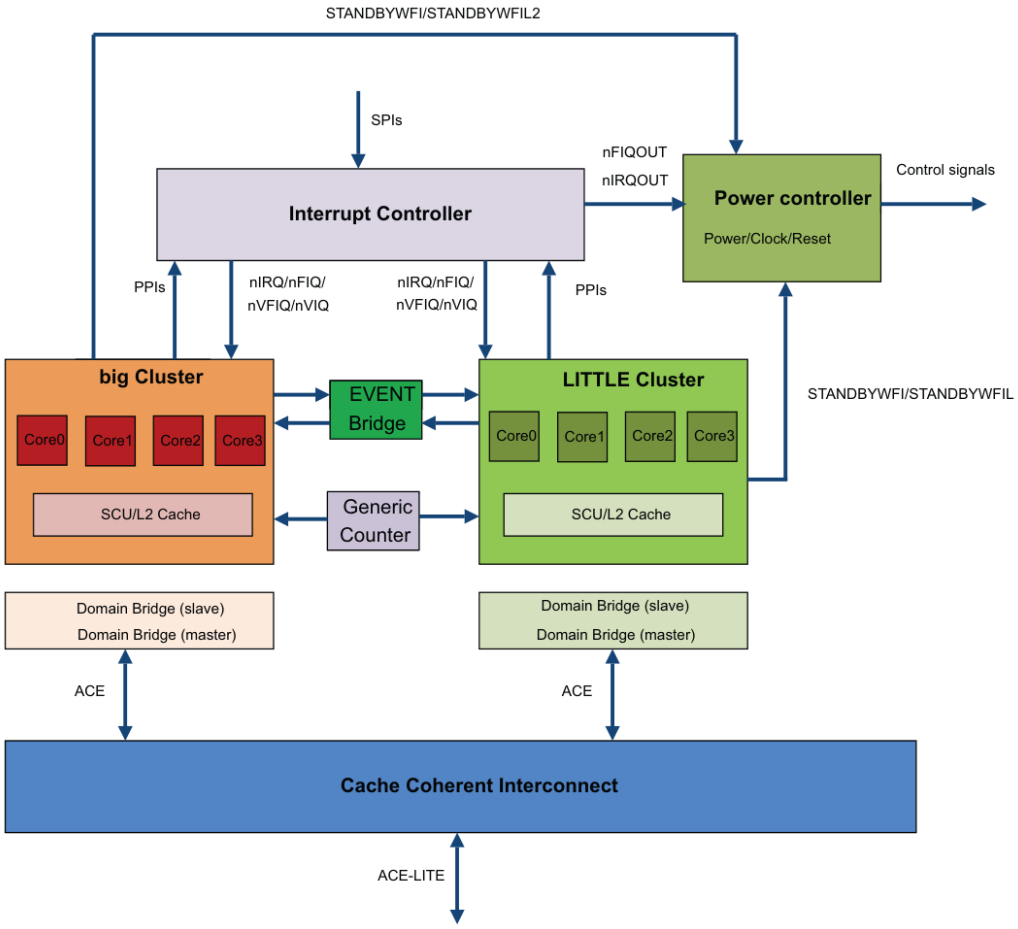
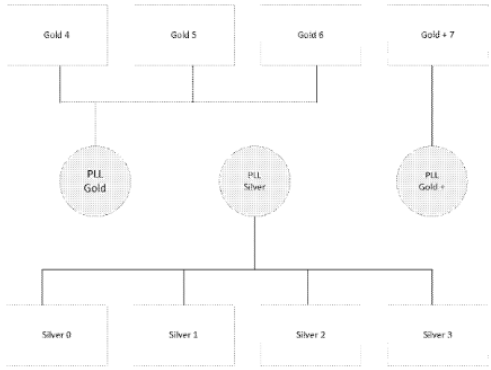
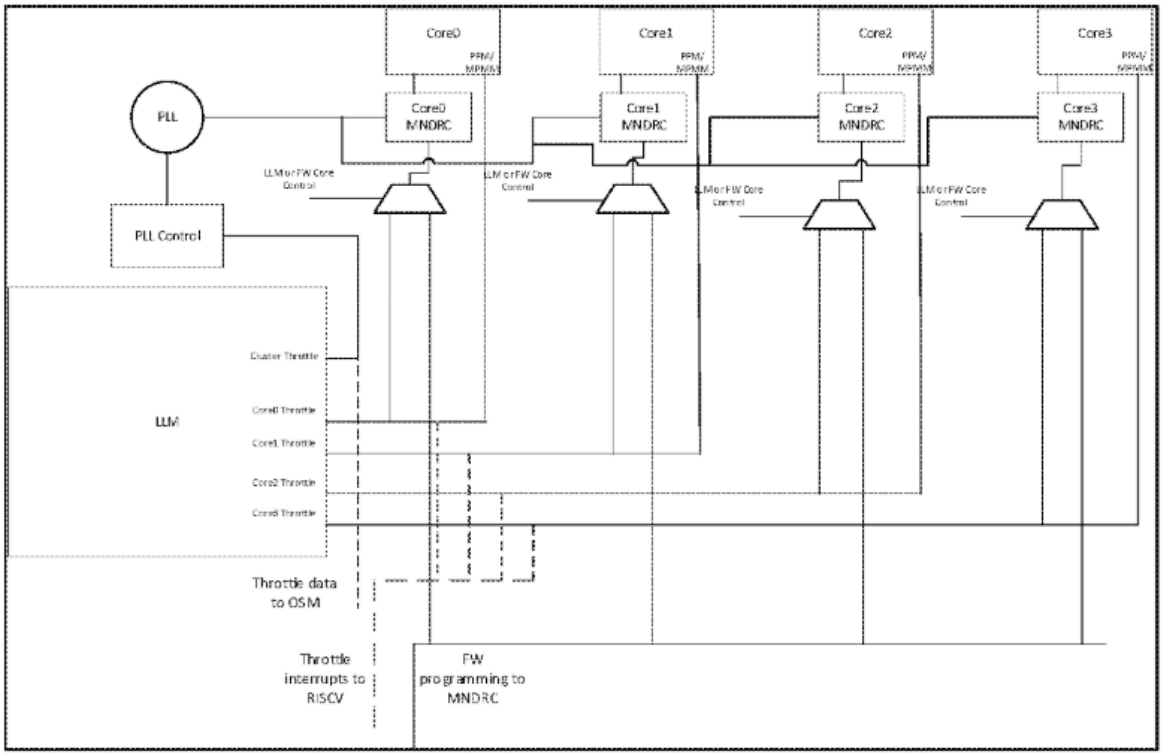


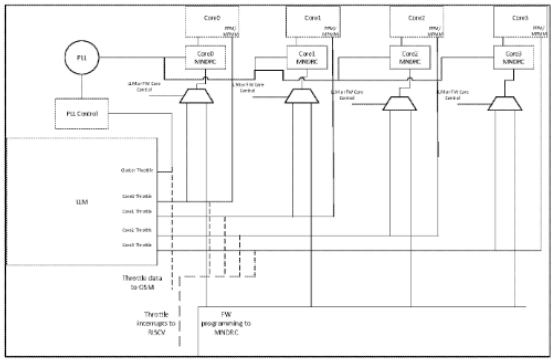
Figure 2-1 A typical big.LITTLE system

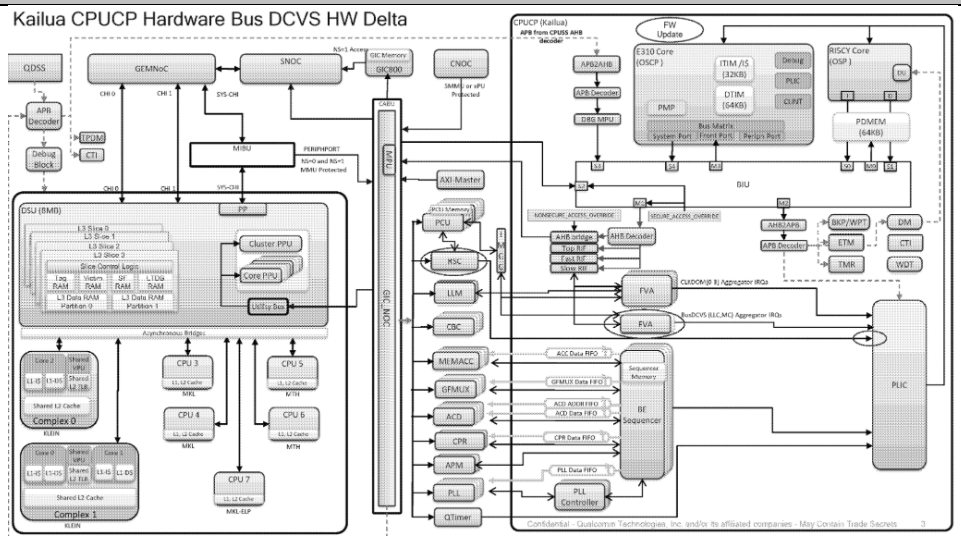
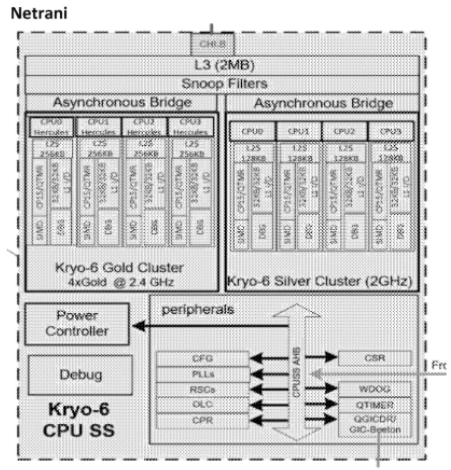
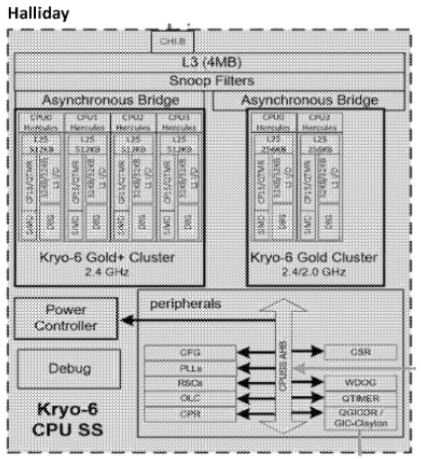
"High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/, at 15 (2-3)

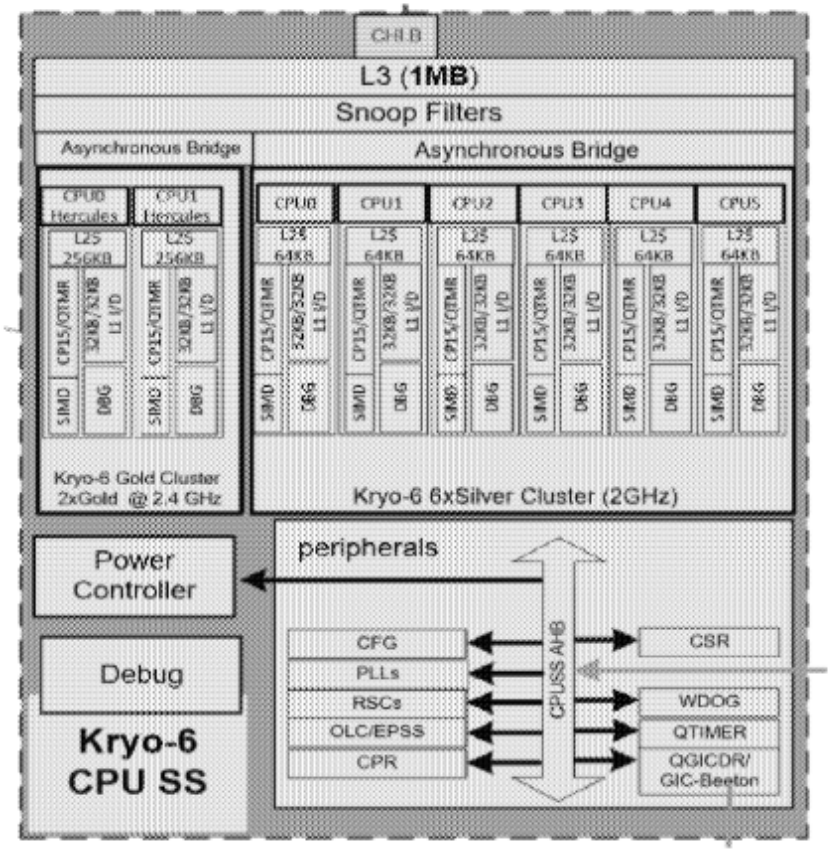
Claim 21	Accused Products
	2.1.1 big cluster and LITTLE cluster This example system uses a big cluster and a LITTLE cluster, and each cluster consists of four cores. There are five power domains for each cluster. Each core is in its own power domain to enable individual powerdown. The rest of the logic within a cluster is in a different power domain. Isolation cells exist between power domains for isolation. Each cluster is implemented in an independent voltage domain with an independent clock source. Each of the clusters has a unique Dynamic Voltage and Frequency Scaling (DVFS) curve. Therefore, cores in the same cluster must traverse an *Operating Performance Point* (OPP) together. You can change the OPP of cores in a cluster, without affecting the cores in the other cluster. *Id.* **2.1.2 Power controller** The power controller contains the hardware power control functions of the SoC. The operations of the power controller are both directed by the *Operating System Power Management* (OSPM) software and hardware events in the system. The power controller works closely with relevant signals of ARM IPs and other system components for power saving. *Id.* Qualcomm's documentation confirms the accused products include the same or similar SCP, PPU, and Power Controller blocks.

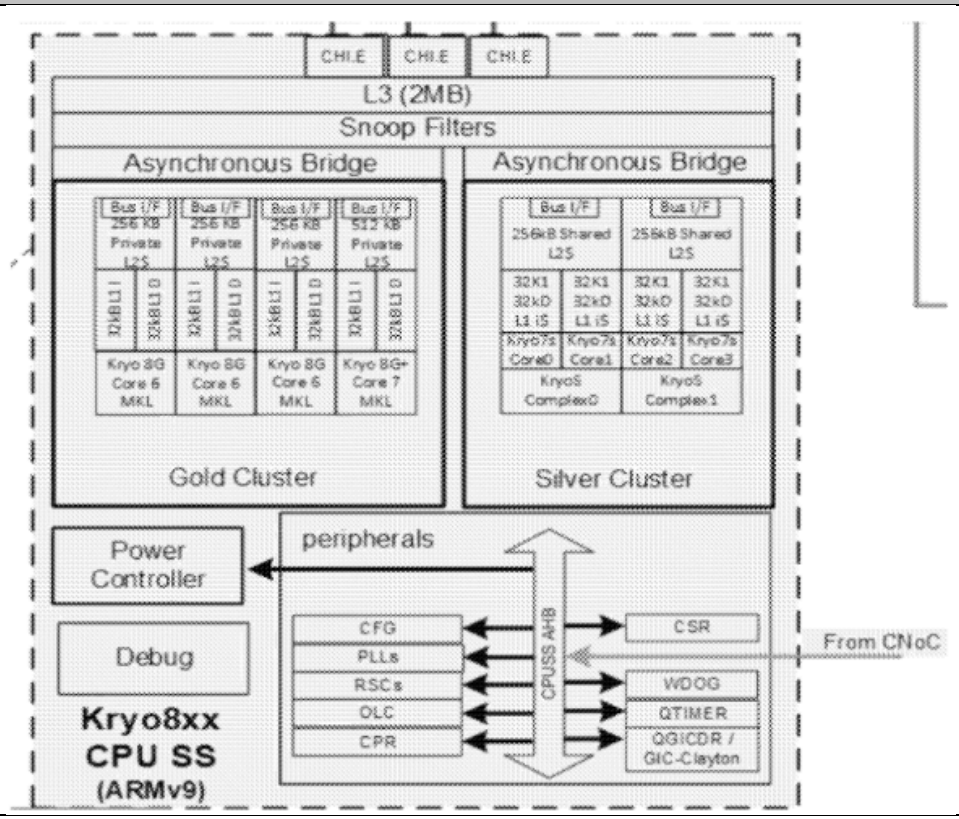
Claim 21	Accused Products
	Motivation Current implementation • Current implementation in CPUSS requires that each core per cluster domain run at the same clock frequency. • This requirement is due to the fact that each core doesn't have its own PLL. • OSM aggregates and chooses MAX frequency for operation for those cores. 

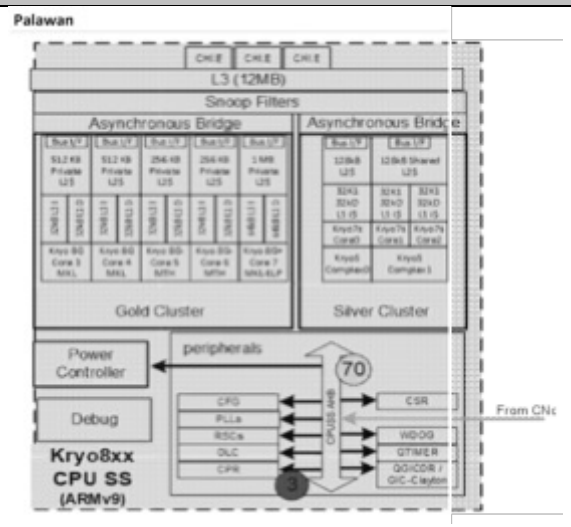
Claim 21	Accused Products
	 Kailua

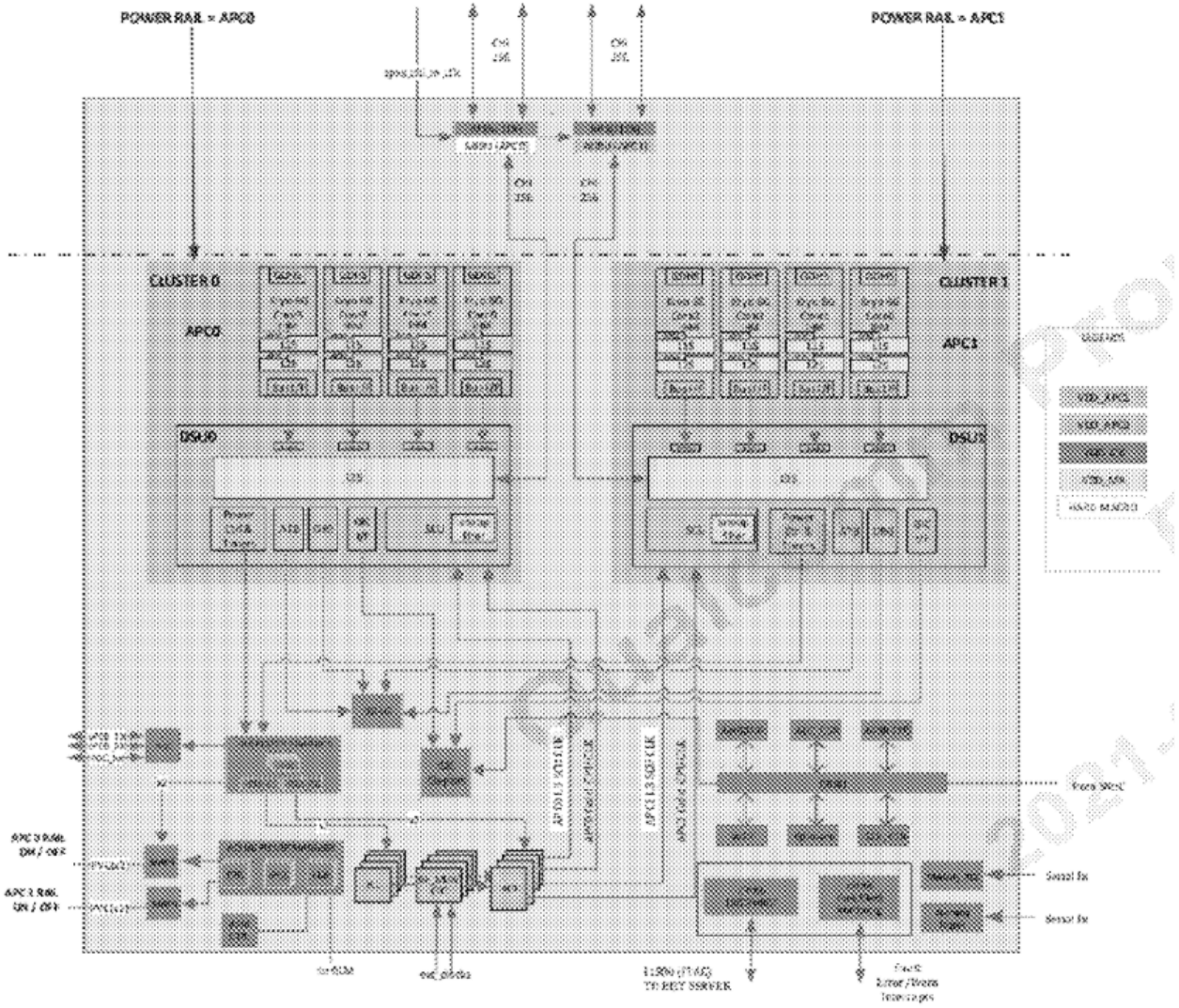
Claim 21	Accused Products
	LLM & FW Interaction • For Kailua implementation the MNDRC's can either be controlled by FW or by LLM directly but not by both. • When testing for LLM thermal mitigation data the MUX control is switched to LLM that will drive per core MVAL based on it's LUT table. • When gathering power profile data for SW the MUX control is switched to FW. • Note that if there is a need to capture data from SW and LLM driven MVAL's to MNDRC then Interrupt driven control is to be used to ensure we have single master that drives MVAL. • Note that POR implementation for inner and outer loop and per core MPMM/PPM control remains the same. • The Design has been introduced such that it does not affect POR requirements of LLM and FW Source sample text 15  QCREDSTONE_0098870 at -74, -83, -84.

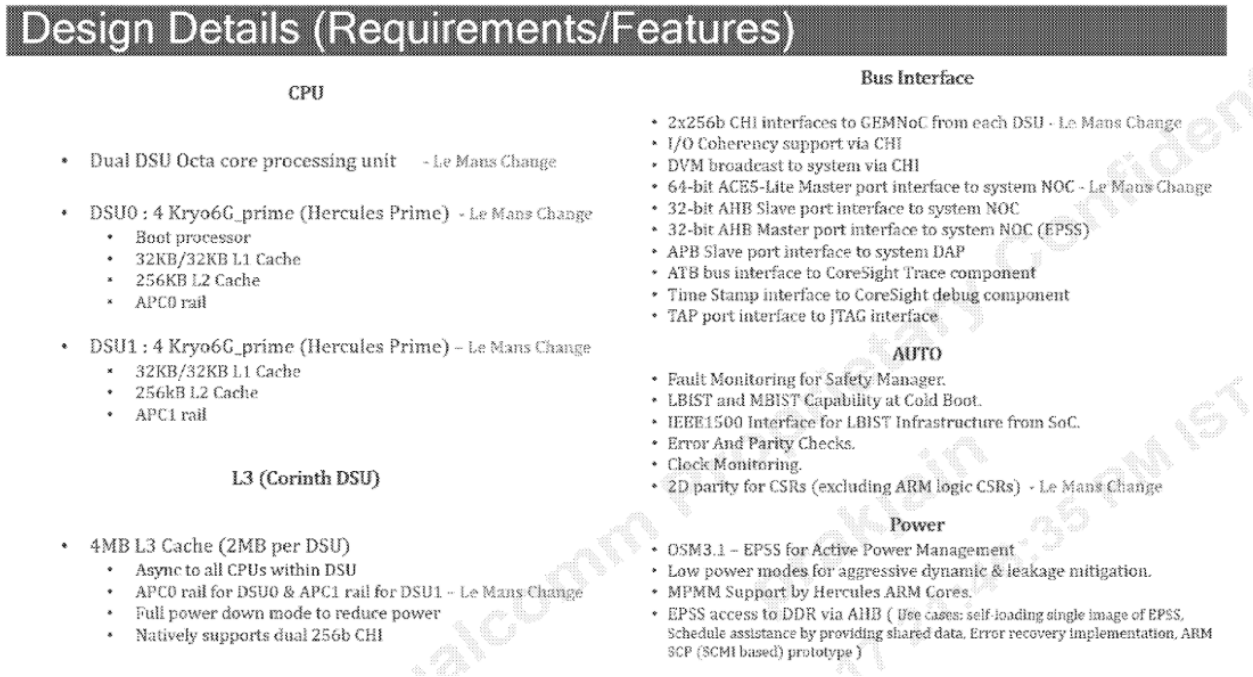
Claim 21	Accused Products
	 QCREDSTONE_0098768 at -70.
	
	

Claim 21	Accused Products
	Clarence 

Claim 21	Accused Products
	

Claim 21	Accused Products
	 QCREDSTONE_0098556 at -558 to -562.

Claim 21	Accused Products
	

Claim 21	Accused Products
	 QCREDSTONE_0091177 at -86-87.
[21b] a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage from the power control block and a second output clock signal from a second PLL having a second clock	Each Accused Product comprises a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage from the power control block and a second output clock signal from a second PLL having a second clock signal as input in the clock control block, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal *See* analysis and evidence of claim element [1b] above. Furthermore, each DynamIQ Accused Product includes a power control block and a clock control block. For example, according to ARM's documents and reference design, the multi-core processor should contain a system control processor (SCP) to control voltage, power, and clocks,

Claim 21	Accused Products
signal as input in the clock control block, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and	and power policy units (PPUs) to manage power states on each voltage domain. On information and belief, each DynamIQ Accused Product contains an SCP and one or more PPUs as described. For another example, according to ARM's documents and reference design, a big.LITTLE multi-core processor should contain a power controller and other controllers for supplying the voltage and clock signals as claimed. On information and belief, each big.LITTLE Accused Product contains a power controller and other controllers as described. *See, e.g.*:

Claim 21	Accused Products

6.1 The Power Policy Unit

Power mode control for the *DynamIQ™ Shared Unit-110* (DSU-110) is provided by the *Power Policy Units* (PPUs) that are integrated into the cluster. These PPUs control all the PPU modes for all components in the cluster.

A PPU is a standard component for abstracting software-controlled power domain policy to low-level hardware control signaling. There is one PPU for controlling the DSU-110 DynamIQ™ cluster power domain (PDCLUSTER). Also, each core has its own individual PPU for controlling its respective core power domain (for example, a PPU for PDCORE0 and a PPU for PDCORE1). This includes any cores included as part of a complex.

A component in the system such as a *System Control Processor* (SCP) can program the PPUs through the utility bus to set the required power policy. The PPUs control the low-level details of powering up, powering down, and resetting domains as necessary to implement the requested policy. The hardware performs any actions to reach the requested power mode, such as gating clocks, cleaning and invalidating caches, or disabling coherency.



- Although the cluster and each core in the cluster has their own PPU, the shared logic of a complex does not have a dedicated PPU. Instead, power management of the complex is controlled as a combination of the PPUs for the cores it contains. See Table 5-8: PPU mode and power domain states for a dual-core complex on page 74.
- The cluster and all the core PPUs are provided as part of the DSU-110.
- The implementation process automatically creates the PPU for the cluster and each core PPU, and connects these into the DSU-110 DynamIQ™ cluster. Each PPU has a set of memory-mapped control registers which is accessed using the utility bus.

Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 78

Claim 21	Accused Products
	4.3 Power control Good power management is key to reduce system power consumption while maintaining a high performance. An RD-TC21 reference subsystem contains the following power management features: • Multiple voltage domains to allow for *Dynamic Voltage and Frequency Scaling* (DVFS) on application processors and the GPU • Multiple power-gated regions provide comprehensive leakage management • Multiple power modes for different system scenarios • A *System Control Processor* (SCP) based on a Cortex®-M3 processor controls power, clock, reset, and the static configuration of the system • *Power Policy Units* (PPUs) are used to manage power states of each voltage and power domain under the control of the SCP Arm® Total Compute 2021 Reference Design Software Developer Guide at 47-48

Claim 21	Accused Products
	SCP runtime firmware The SCP runtime firmware executes after *Trusted Firmware for A-profile* (TF-A) BL2 has authenticated and copied it from flash. The SCP runtime firmware performs the following functions: • Responds to *System Control and Management Interface* (SCMI) messages through *Message Handling Unit* (MHU) version 2.0 for processor power control and *Dynamic Voltage and Frequency Scaling* (DVFS) • Power domain management • Clock management *Id.* at p. 65

Claim 21	Accused Products

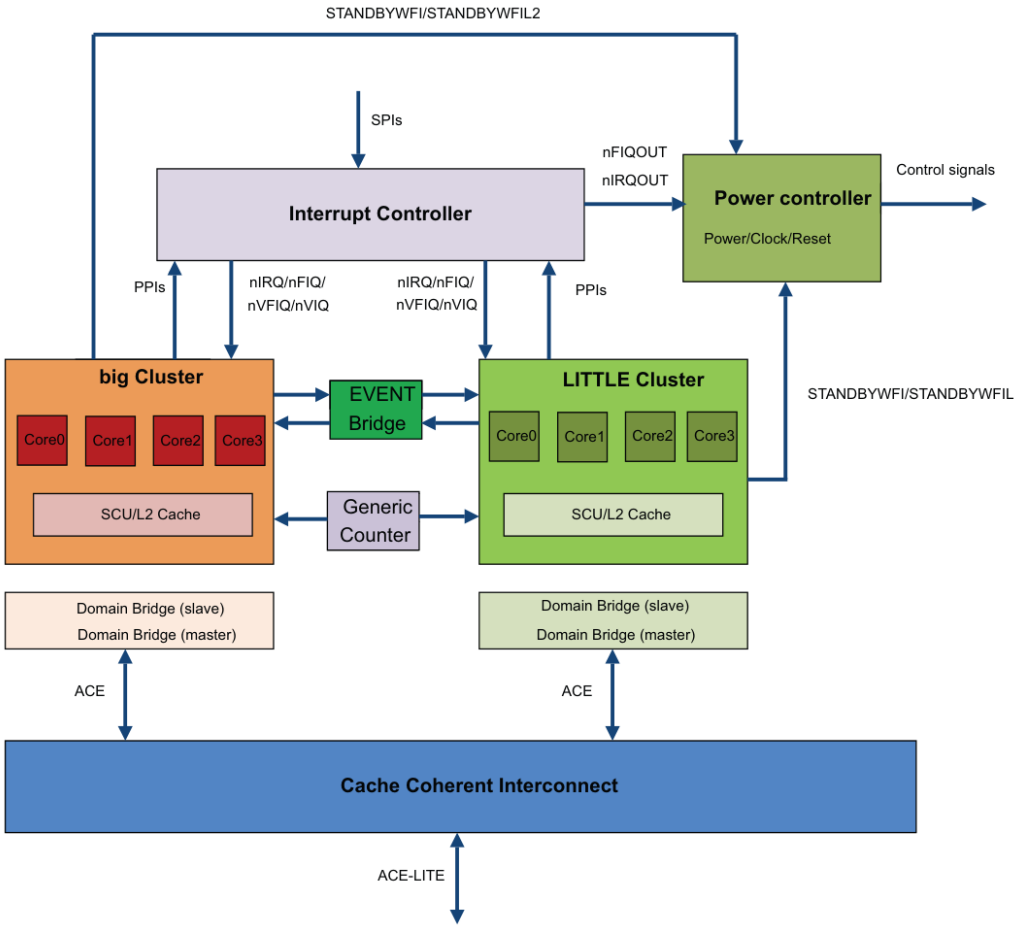
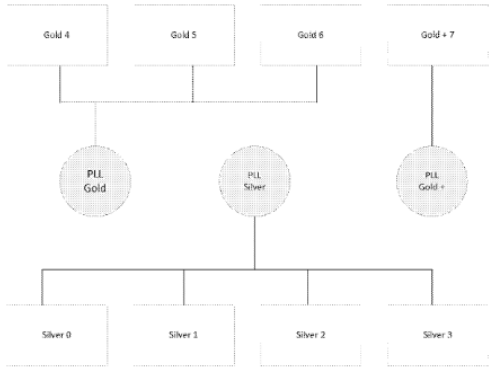
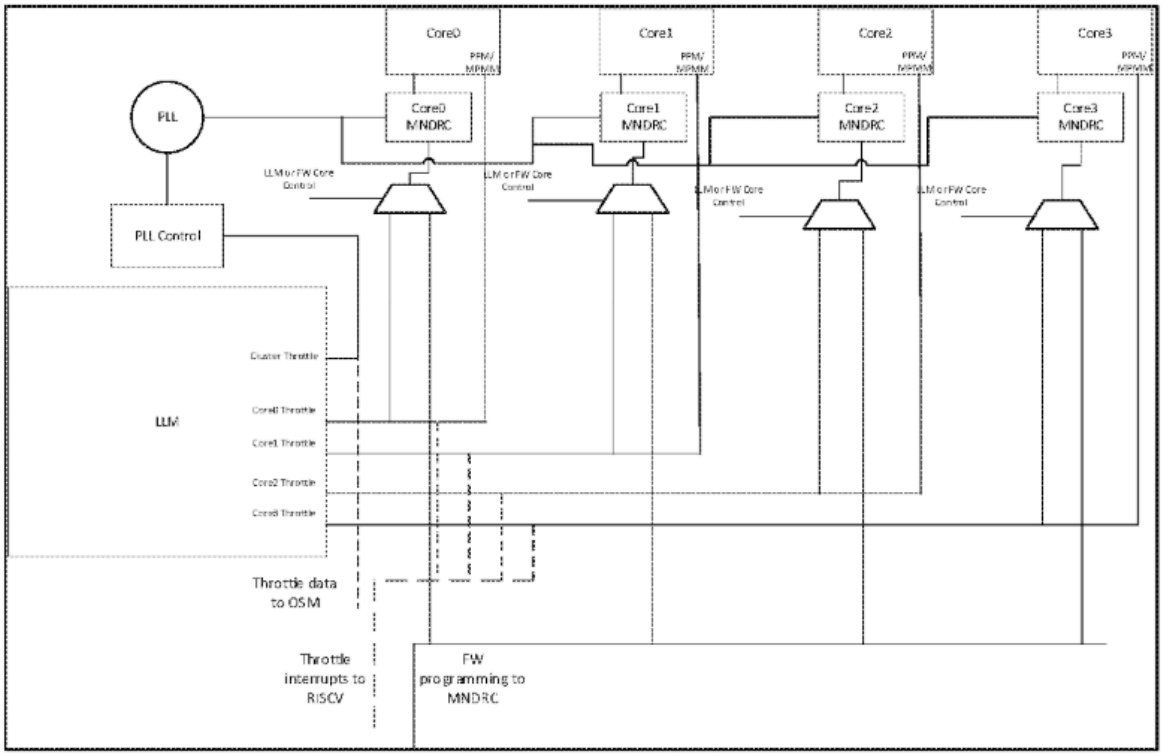


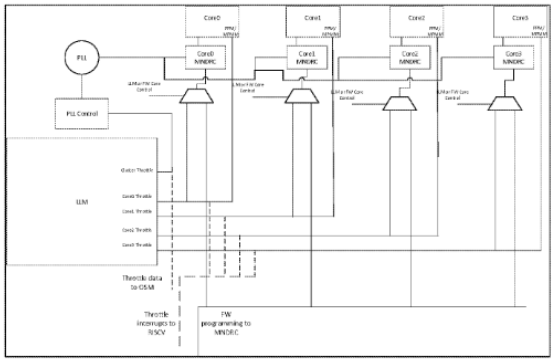
Figure 2-1 A typical big.LITTLE system

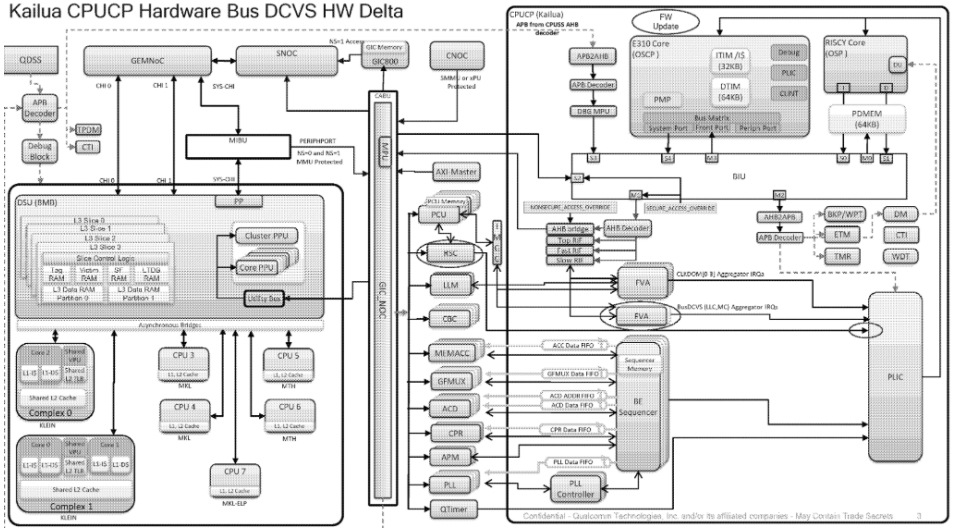
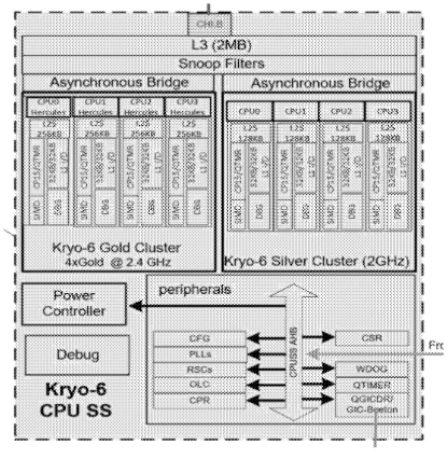
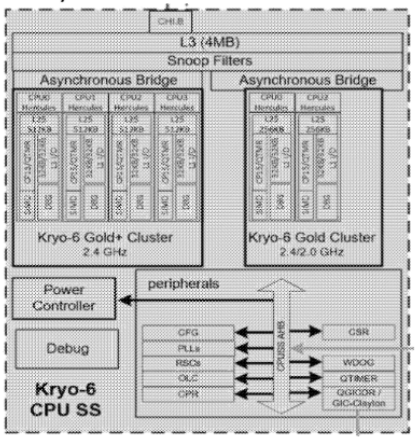
"High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/, at 15 (2-3)

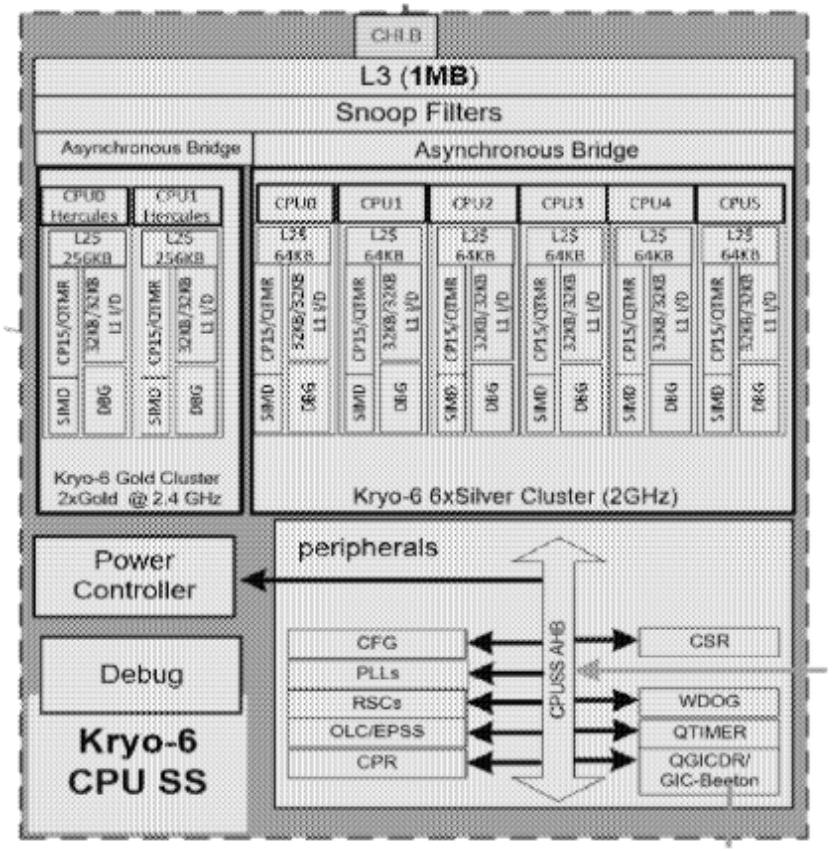
Claim 21	Accused Products
	2.1.1 big cluster and LITTLE cluster This example system uses a big cluster and a LITTLE cluster, and each cluster consists of four cores. There are five power domains for each cluster. Each core is in its own power domain to enable individual powerdown. The rest of the logic within a cluster is in a different power domain. Isolation cells exist between power domains for isolation. Each cluster is implemented in an independent voltage domain with an independent clock source. Each of the clusters has a unique Dynamic Voltage and Frequency Scaling (DVFS) curve. Therefore, cores in the same cluster must traverse an *Operating Performance Point* (OPP) together. You can change the OPP of cores in a cluster, without affecting the cores in the other cluster. *Id.* **2.1.2 Power controller** The power controller contains the hardware power control functions of the SoC. The operations of the power controller are both directed by the *Operating System Power Management* (OSPM) software and hardware events in the system. The power controller works closely with relevant signals of ARM IPs and other system components for power saving. *Id.* Qualcomm's documentation confirms the accused products include the same or similar SCP, PPU, and Power Controller blocks.

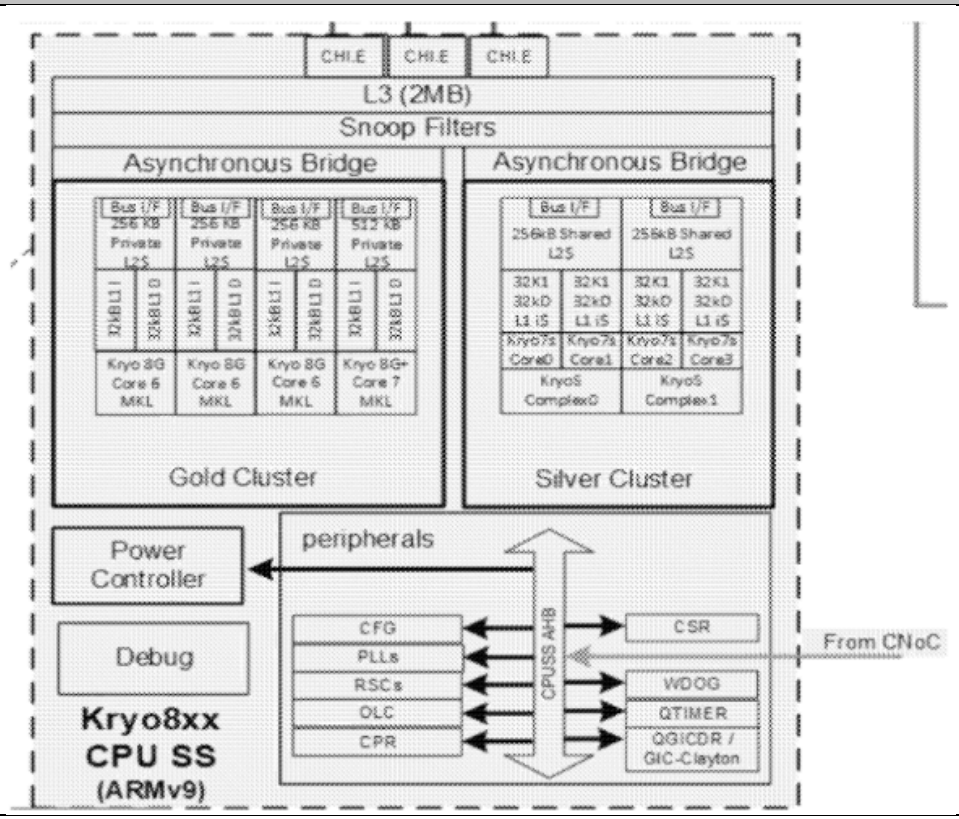
Claim 21	Accused Products
	Motivation Current implementation • Current implementation in CPUSS requires that each core per cluster domain run at the same clock frequency. • This requirement is due to the fact that each core doesn't have its own PLL. • OSM aggregates and chooses MAX frequency for operation for those cores. 

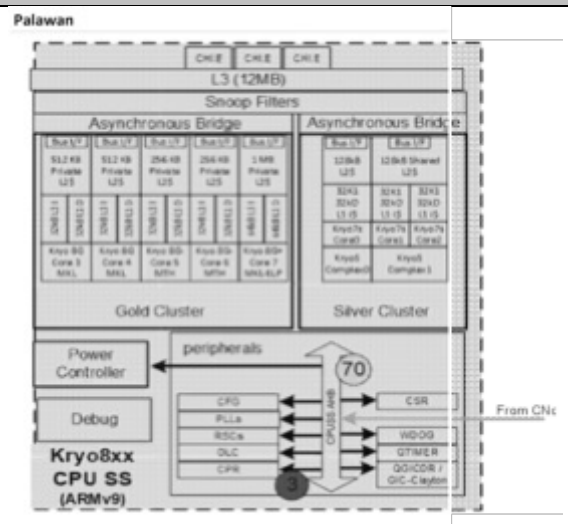
Claim 21	Accused Products
	 Kailua

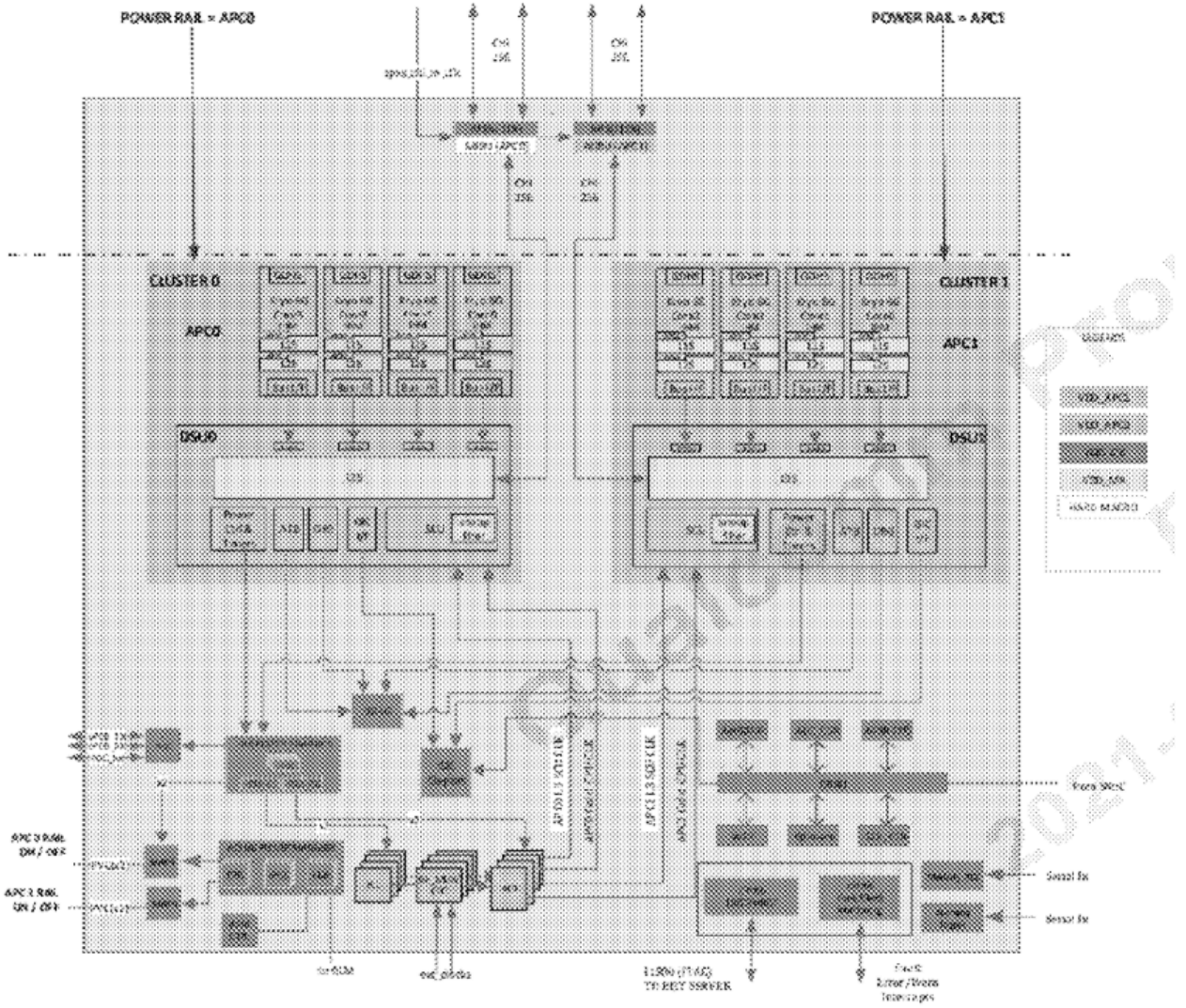
Claim 21	Accused Products
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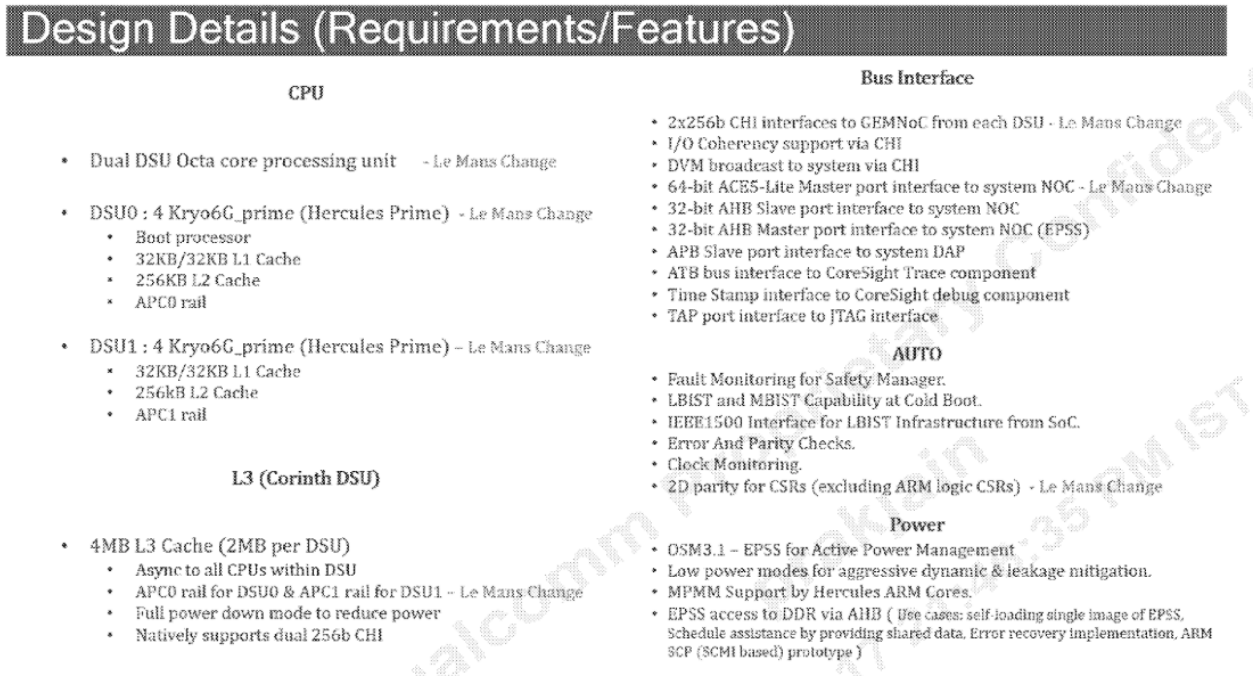
Claim 21	Accused Products
	Kailua CPUCP Hardware Bus DCVS HW Delta  QCREDSTONE_0098768 at -70. Netrani  Halliday 

Claim 21	Accused Products
	Clarence 

Claim 21	Accused Products
	

Claim 21	Accused Products
	 QCREDSTONE_0098556 at -558 to -562.

Claim 21	Accused Products
	

Claim 21	Accused Products
	 QCREDSTONE_0091177 at -86-87.
[21c] an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.	Each Accused Product comprises an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores. *See* analysis and evidence of claim element [1c] above.